1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SAFFORO_MLB,SCHEM

| REV | ECN | DESCRIPTION OF REVISION | CK APPD / DATE |
|---|---|---|---|
| 4 | 0011084277 | ENGINEERING RELEASED | 2018-04-20 |

LAST_MODIFICATION=Fri Apr 20 15:11:56 2018


| PAGE | CSA | CONTENTS | SYNC | DATE |
|---|---|---|---|---|
| 1 | 1 | Table of Contents | SAFFORO | 05/24/2017 |
| 2 | 2 | BOM Configuration 1 | SAFFORO | 11/29/2017 |
| 3 | 3 | BOM Configuration 2 | SAFFORO | 11/29/2017 |
| 4 | 4 | PD Parts | ZIFENG_CONSTRAINTS | 03/03/2017 |
| 5 | 5 | CPU DMI/PEG/FDI/RSVD | ZIFENG | 09/07/2017 |
| 6 | 6 | CPU Clock/Misc/JTAG/CFG | Giordano_mlb | 11/11/2017 |
| 7 | 7 | CPU DDR4 Interfaces | Giordano_mlb | 11/11/2017 |
| 8 | 8 | CPU Power | ZIFENG_CONSTRAINTS | 02/24/2017 |
| 9 | 9 | CPU Ground | Giordano_mlb | 11/11/2017 |
| 10 | 10 | CPU Decoupling 1 | SILU | 03/29/2017 |
| 11 | 11 | CPU Decoupling 2 | SILU | 05/24/2017 |
| 12 | 12 | PCH RTC/CLK/ESPI/PM | ZIFENG | 05/18/2017 |
| 13 | 13 | PCH DMI/JTAG/SPI/HDA | SILU | 07/27/2017 |
| 14 | 14 | PCH PCI-E/USB | ZIFENG | 05/18/2017 |
| 15 | 15 | PCH GPIO/MISC/NCTF | ZIFENG | 05/18/2017 |
| 16 | 16 | PCH Power | ZIFENG | 05/18/2017 |
| 17 | 17 | PCH Decoupling | ZIFENG | 05/18/2017 |
| 18 | 18 | CPU/PCH Merged XDP | ZIFENG | 05/24/2017 |
| 19 | 19 | Chipset Support 1 | SILU | 08/09/2017 |
| 20 | 20 | Chipset Support 2 | ZIFENG | 05/18/2017 |
| 21 | 22 | DDR4 VREF Margining | Giordano_mlb | 11/11/2017 |
| 22 | 23 | DDR4 SDRAM Channel A 1 | Giordano_mlb | 11/11/2017 |
| 23 | 24 | DDR4 SDRAM Channel A 2 | Giordano_mlb | 11/11/2017 |
| 24 | 25 | DDR4 SDRAM Channel B 1 | Giordano_mlb | 11/11/2017 |
| 25 | 26 | DDR4 SDRAM Channel B 2 | Giordano_mlb | 11/11/2017 |
| 26 | 27 | DDR4 Termination | Giordano_mlb | 11/11/2017 |
| 27 | 28 | USB-C HIGH SPEED 1 | J132 | 05/11/2017 |
| 28 | 29 | USB-C HIGH SPEED 2 | ADITYA | 03/30/2017 |
| 29 | 30 | USB-C X Support | ADITYA | 04/19/2017 |
| 30 | 31 | USB-C PORT CONTROLLER A | ZIFENG | 05/26/2017 |
| 31 | 32 | USB-C PORT CONTROLLER B | ZIFENG | 05/26/2017 |
| 32 | 33 | USB-C CONNECTOR A | SILU_J680 | 08/09/2017 |
| 33 | 34 | USBC X Connector Support | ADITYA | 04/05/2017 |
| 34 | 35 | TBT 5V REGULATOR | J132 | 04/05/2017 |
| 35 | 36 | WIFI/BT: Support | J132 | 03/29/2017 |
| 36 | 37 | WIFI/BT: MODULE 1 | METE | 05/10/2017 |
| 37 | 38 | AP & BT Conn | METE | 08/11/2017 |
| 38 | 39 | SoC GPIO/SEP/USB/DDR/Test | SILU | 05/26/2017 |
| 39 | 40 | SoC AOP/AON/SMC | SILU | 03/22/2017 |
| 40 | 41 | SoC ISP/I2C/UART/SPI/I2S | H9M and PMIC | 03/02/2017 |
| 41 | 42 | SoC PCIe | SILU | 03/15/2017 |
| 42 | 43 | SoC Power 1 | SILU | 04/04/2017 |
| 43 | 44 | SoC Power 2 | H9M and PMIC | 03/02/2017 |
| 44 | 45 | SoC Power 3 | SILU | 05/26/2017 |
| 45 | 46 | SoC Ground | H9M and PMIC | 03/02/2017 |
| 46 | 47 | SoC Shared Support | SILU | 08/09/2017 |
| 47 | 48 | SoC Project Support | SILU | 07/27/2017 |
| 48 | 49 | MESA | SILU | 05/26/2017 |
| 49 | 50 | Secure Element | SILU | 05/05/2017 |
| 50 | 51 | DFR & T208 Support | SILU | 07/27/2017 |
| 51 | 52 | I2C Connections 1 | RAYMOND | 10/02/2017 |
| 52 | 53 | I2C Connections 2 | RAYMOND | 10/02/2017 |
| 53 | 54 | Power Sensors High Side | RAYMOND | 10/09/2017 |
| 54 | 55 | Power Sensors Load Side | RAYMOND | 10/13/2017 |
| 55 | 56 | Power Sensors Extended 1 | RAYMOND | 10/13/2017 |
| 56 | 57 | Power Sensors Extended 2 | RAYMOND | 10/13/2017 |
| 57 | 58 | Thermal Sensors | RAYMOND | 06/28/2017 |
| 58 | 59 | Power Sensor Extended 3 | RAYMOND | 10/13/2017 |
| 59 | 60 | Fans/SMC/AMUX Support | RAYMOND | 06/13/2017 |
| 60 | 62 | Audio Placeholder | j132-audio | 03/15/2017 |
| 61 | 63 | Audio Jack Codec | TROY | 07/24/2017 |
| 62 | 64 | Audio Left Amplifiers | TROY | 12/11/2017 |
| 63 | 65 | Audio Right Amplifiers | TROY | 12/11/2017 |
| 64 | 66 | Audio Flex Connectors | TROY | 03/22/2017 |
| 65 | 67 | Keyboard & Trackpad 1 | j132 | 03/23/2017 |
| 66 | 68 | Keyboard & Trackpad 2 | j132 | 03/23/2017 |
| 67 | 69 | VR 3.3V G3H & Battery Conn | SILU | 04/27/2017 |
| 68 | 70 | PBUS Supply & Battery Charger | ZIFENG | 05/24/2017 |
| 69 | 71 | IMVP IC | SILU | 05/24/2017 |
| 70 | 72 | IMVP VCC Block | SILU | 05/24/2017 |
| 71 | 73 | IMVP SA Block | SILU | 05/10/2017 |
| 72 | 74 | IMVP GT Block | SILU | 05/24/2017 |
| 73 | 76 | Power - 5V 3.3V Supply | SILU | 05/16/2017 |
| 74 | 77 | VR 2.5V & 1.2V/VTT | SILU | 05/01/2017 |
| 75 | 78 | PMIC BUCKS AND SWs | SILU | 06/06/2017 |
| 76 | 79 | PMIC LDOs | SILU | 07/10/2017 |
| 77 | 80 | PMIC GPIOs & Control | SILU | 07/27/2017 |
| 78 | 81 | VR VCCIO | SILU | 05/10/2017 |
| 79 | 82 | Power FETs | SILU | 06/27/2017 |
| 80 | 83 | SOC/PMIC Aliases | SILU | 08/09/2017 |
| 81 | 84 | LCD Backlight Driver | RAYMOND | 08/07/2017 |
| 82 | 85 | eDP Display Connector | SEAN | 08/09/2017 |
| 83 | 86 | SSD0 S4E 0 | j137_gm5_redhead | 01/26/2017 |
| 84 | 87 | SSD0 S4E 1 | j137_gm5_redhead | 01/26/2017 |
| 85 | 88 | SSD0 S4E 2 | j137_gm5_redhead | 01/26/2017 |
| 86 | 89 | SSD0 S4E 3 | j137_gm5_redhead | 01/26/2017 |
| 87 | 90 | SSD0 PMIC & VR | j137_gm5_redhead | 01/26/2017 |
| 88 | 91 | SSD1 S4E 0 | j137_gm5_redhead | 01/26/2017 |
| 89 | 92 | SSD1 S4E 1 | j137_gm5_redhead | 01/26/2017 |
| 90 | 93 | SSD1 S4E 2 | j137_gm5_redhead | 01/26/2017 |
| 91 | 94 | SSD1 S4E 3 | | |
| 92 | 95 | SSD1 PMIC & VR | | |
| 93 | 98 | EDP Mux | SEAN | 05/01/2017 |
| 94 | 99 | GPU PCC | SEAN | 11/09/2017 |
| 95 | 100 | GPU Baffin PCIe | SEAN | 11/09/2017 |
| 96 | 101 | GPU Baffin Core/FB Power | SEAN | 06/21/2017 |
| 97 | 102 | GPU Baffin FB | SEAN | 04/19/2017 |
| 98 | 103 | VR 1.05V GPU & 1.35V FB | SILU | 04/27/2017 |
| 99 | 104 | GDDR5 VRAM FB 1 [104] | SEAN | 04/19/2017 |
| 100 | 105 | GDDR5 VRAM FB 2 | SEAN | 04/19/2017 |
| 101 | 106 | VR GPU Core | SILU | 05/24/2017 |
| 102 | 107 | GPU Baffin GPIO/CLK/Straps | SEAN | 04/19/2017 |
| 103 | 108 | GPU Baffin DP/GPIO | SILU | 07/27/2017 |
| 104 | 109 | GPU Baffin VSS/Misc | SEAN | 11/09/2017 |
| 105 | 110 | USB-C HIGH SPEED 1 | J132 | 05/11/2017 |
| 106 | 111 | USB-C HIGH SPEED 2 | ADITYA | 04/03/2017 |
| 107 | 112 | USB-C T Support | ADITYA | 04/19/2017 |
| 108 | 113 | USB-C PORT CONTROLLER A | ZIFENG | 05/26/2017 |
| 109 | 114 | USB-C PORT CONTROLLER B | ZIFENG | 05/26/2017 |
| 110 | 115 | USB-C CONNECTOR A | SILU_J680 | 08/09/2017 |
| 111 | 116 | USBC T Connector Support | ADITYA | 04/05/2017 |
| 112 | 117 | USB-C T 5V VR | SILU | 05/11/2017 |
| 113 | 118 | GDDR5 VRAM FB 3 | j680_copy | 02/01/2017 |
| 114 | 119 | GDDR5 VRAM FB 4 | j680_copy | 02/01/2017 |
| 115 | 120 | Power Alias 1 | SILU | 05/01/2017 |
| 116 | 121 | Power Alias 2 | SILU | 06/27/2017 |
| 117 | 122 | Signal Alias | METE | 05/10/2017 |
| 118 | 123 | High speed No Testpoints | RAYMOND | 06/02/2017 |
| 119 | 124 | DFU TEST POINTS | RAYMOND | 08/07/2017 |
| 120 | 125 | FCT TESTPOINTS 2 | RAYMOND | 08/07/2017 |
| 121 | 126 | ICT, MAC-1 ,BE Testpoints | RAYMOND | 08/31/2017 |
| 122 | 127 | Desense Caps 1 | SEAN | 06/27/2017 |
| 123 | 128 | Desense Caps 2 | j380_mlb | 02/09/2017 |
| 124 | 129 | Desense Caps 3 | blah | 06/27/2017 |
| 125 | 130 | Memory Bite/Byte Swizzle | j380_mlb | 02/09/2017 |
| 126 | 140 | Dev Support | Debug | 05/03/2017 |
| 127 | 141 | Blank | | 11/11/2017 |
| 128 | 143 | Blank | | 11/11/2017 |
| 129 | 144 | Blank | | 11/11/2017 |
| 130 | 147 | BOM Alt Table | SEAN | 11/29/2017 |
| 131 | 200 | Dev Support | ADITYA | 03/22/2017 |


# Preliminary Test

Schematic / PCB #'s

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-02888 | 1 | SCH,MLB,SAFFORO | SCH | CRITICAL | FAB#:RC315 |
| 820-01814 | 1 | PCBF,MLB,SAFFORO | PCB | CRITICAL | FAB#:RC315 |
| | | | | | |

FAB#:RC315

DRAWING TITLE: SCHEM,MLB,SAFFORO

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0

BRANCH: EVT

PAGE: 1 OF 200

SHEET: 1 OF 131


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## SAFFORO BOM Groups

| BOM GROUP | BOM OPTIONS |
|---|---|
| SAFFORO_8L | ALTERNATE,S4E_L5,S4E_L6,S4E_L7,S4E_L8,OCARINA_2,S4E_X4PLUS,S4E_X8 |
| SAFFORO_6L | ALTERNATE,S4E_L5,S4E_L6,OCARINA_2,S4E_X4PLUS,S4E_X6 |
| SAFFORO_COMMON | SCH,PCB,COMMON,ALTERNATE,SAFFORO_COMMON1,SAFFORO_COMMON2,SAFFORO_PROGPARTS,VRAM_ALTS |
| SAFFORO_COMMON1 | CPUPEG:X8X4X4,EDP:YES,BOARD_ID,BOARD_REV:011,SE:PROD_2017,EN_VP0R_LPS:YES |
| SAFFORO_COMMON2 | SKIP_5V3V3:AUDIBLE,XDP:YES,SYSDET:PET,VCCSPI:3V3,OCARINA_I2C:1X,SVID_PU:CORE,RF_TUNING,PEUS:3S |
| SAFFORO_PROGPARTS | UPCROM_PROG:P1,WIFI_ROM:P0,BT_ROM:P2 |
| SAFFORO_SNS | LOADISNS,LOADRC:YES,SENSOR:DEV |
| SAFFORO_DEVEL:ENG | ALTERNATE,SAFFORO_SNS,DEBLID,EDP_CORE,PEUS_ENG,PPG_ENG,VIPZ_ENG,DBG_PAR,GPUROM:BLASE,TEMPS0-7:YES,PCI:YES,GPU_ROM:DEE,BOOTGPU |
| SAFFORO_DEVEL:DVT | ALTERNATE,LOADRC:NO |
| SAFFORO_DEVEL:PVT | ALTERNATE,LOADRC:NO |

## BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 685-00234 | COMMON PARTS,MLB,SAFFORO | SAFFORO_COMMON |
| 685-00314 | S4E 8L Parts,MLB,SAFFORO | SAFFORO_8L |
| 685-00318 | S4E 6L Parts,MLB,SAFFORO | SAFFORO_6L |
| 985-00421 | DEV,MLB,SAFFORO | SAFFORO_DEVEL:ENG |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 685-00234 | 1 | COMMON PARTS, MLB, SAFFORO | BASE | CRITICAL | BASE_BOM |
| 685-00314 | 1 | S4E 8L PARTS (8L),MLB,SAFFORO | 8L | CRITICAL | BOM_8L |
| 985-00421 | 1 | DEV PARTS,MLB,SAFFORO | DEVEL | CRITICAL | DEVEL_BOM |
| 685-00318 | 1 | S4E 6L PARTS (6L),MLB,SAFFORO | 6L | CRITICAL | BOM_6L |

## VRAM ALT BOM GROUPS

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 685-00221 | VRAM PARTS,HYNIX,2X,MLB,SAFFORO | FB_4GB_HYNIX |
| 685-00222 | VRAM PARTS,MICRON,2X,MLB,SAFFORO | FB_4GB_MICRON |
| 685-00223 | VRAM PARTS,SAMSUNG,2X,MLB,SAFFORO | FB_4GB_SAMSUNG |
| 685-00224 | VRAM PARTS,HYNIX,1Z,MLB,SAFFORO | FB_4GB_HYNIX_1Z |
| 685-00225 | VRAM PARTS,MICRON,1Z,MLB,SAFFORO | FB_4GB_MICRON_1Z |

## VRAM SUB-BOM

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 685-00221 | 1 | VRAM PARTS,HYNIX,2X,MLB,SAFFORO | VRAMSSSS | CRITICAL | VRAM_ALTS |

## DRAM Options

| BOM GROUP | BOM OPTIONS |
|---|---|
| MC_32G | 32G_MICRON_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L |
| HY_32G | 32G_HYNIX_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L |
| HY_16G | 16G_HYNIX_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L,RAMCFG0:L |
| MC_16G | 16G_MICRON_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L |

## S4E Options

| BOM GROUP | BOM OPTIONS |
|---|---|
| TS_256_PMLC | S4E_256_TS,SOC:1GB,SSD0_NAND_VCC:2.5V |
| WD_256_PMLC | S4E_256_WD,SOC:1GB,SSD0_NAND_VCC:2.5V |
| TS_512_PMLC | S4E_512_TS,SOC:1GB,SSD0_NAND_VCC:2.5V |
| WD_512_PMLC | S4E_512_WD,SOC:1GB,SSD0_NAND_VCC:2.5V |
| TS_1TB_PMLC | S4E_1TB_TS,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| WD_1TB_PMLC | S4E_1TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| TS_2TB_PMLC | S4E_2TB_TS,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| WD_2TB_PMLC | S4E_2TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| SM_2TB_3DV4 | S4E_2TB_SM,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| SM_4TB_3DV4 | S4E_4TB_SM,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| TS_2TB_TLC | TLC_2TB_TS,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |
| WD_2TB_TLC | TLC_2TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V |

## BOARD ID

| BOM GROUP | BOM OPTIONS |
|---|---|
| BOARD_ID | BOARDID0,BOARDID1,BOARDID3 |

FAB#:RC315

PAGE TITLE
BOM Configuration 1

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 2 OF 200
SHEET 2 OF 131

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## GPU Baffin

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S00493 | 1 | GPU,AMD,BAFFIN,ULX,A3,0.81,QS,BGA769 | UA000 | CRITICAL | BAFFIN_ULX |
| 337S00494 | 1 | GPU,AMD,BAFFIN,PROX,A3,0.83,QS,BGA769 | UA000 | CRITICAL | BAFFIN_PROX |
| 998-04866 | 1 | INTERPOSER,AMD,C948,BGA769,VDDCI/MVDD | UA000 | CRITICAL | STARDUST:VDDCI_MVDD |
| 998-04867 | 1 | INTERPOSER,AMD,C948,BGA769,VDDC | UA000 | CRITICAL | STARDUST:VDDC |

## FB VDRAM Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 333S00074 | 4 | IC,GDDR5,8Gb,700ps,1.5V,256M,B,170 BGA | UA450,UA450,UA450,UA450 | CRITICAL | FB_4GB_SAMSUNG |
| 333S00075 | 4 | IC,GDDR5,8Gb,700ps,1.5V,256M,A,170 BGA | UA450,UA450,UA450,UA450 | CRITICAL | FB_4GB_MICRON |
| 333S00100 | 4 | IC,GDDR5,8Gb,700ps,1.5V,256M,A,170 BGA | UA450,UA450,UA450,UA450 | CRITICAL | FB_4GB_HYNIX |
| 333S00173 | 4 | IC,GDDR5,8Gb,700ps,1.5V,128M,A,170 BGA | UA450,UA450,UA450,UA450 | CRITICAL | FB_4GB_MICRON_1Z |
| 333S00175 | 4 | IC,GDDR5,8Gb,700ps,1.5V,128M,A,170 BGA | UA450,UA450,UA450,UA450 | CRITICAL | FB_4GB_HYNIX_1Z |

## CPU Parts CFL (Needs to be updated)

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S00571 | 1 | CPU,CFL-H,i9-8950HK,2.9,45W,1.1,BGA1440 | U0500 | CRITICAL | CPU_CFL:2.3 |
| 337S00575 | 1 | CPU,CFL-H,i9-8750H,2.6,45W,1.2,BGA1440 | U0500 | CRITICAL | CPU_CFL:2.6 |
| 337S00587 | 1 | CPU,CFL-H,i9-9980HK,2.4,45W,1.1,BGA1440 | U0500 | CRITICAL | CPU_CFL:2.4 |
| 998-12472 | 1 | INTERPOSER,CFL-H,BGA1440 | U0500 | CRITICAL | CPU_SKL:SOCKET |

## Main DRAM Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 333S00131 | 16 | IC,DDR4M,DDR4-2400,16GB(2),200M,BGA78 | ---------- | CRITICAL | 32G_MICRON_2400 |
| 333S00134 | 16 | IC,DDR4M,DDR4-2400,16GB(2),200M,BGA78 | ---------- | CRITICAL | 32G_HYNIX_2400 |
| 333S00147 | 16 | IC,DDR4M,DDR4-2400,8GB(2),200M,BGA78 | ---------- | CRITICAL | 16G_HYNIX_2400 |
| 333S00163 | 16 | IC,DDR4M,DDR4-2400,8GB(2),200M,BGA78 | ---------- | CRITICAL | 16G_MICRON_2400 |

## PCH CNL-H (Needs to be updated)

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S00523 | 1 | IC,CNL,PCH-H,USTF,QHV9,QS,BO,BGA499 | U1200 | CRITICAL | |

## ACE & Ridges (Needs to Be Updated)

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S01442 | 4 | IC,CD3215,ACE,CS,USB PWR SW,BLBK,DQ196 | U3100,U3200,U3300,U3400 | CRITICAL | |
| 338S00408 | 2 | IC,TSC,TITAN RIDGE DP,QATE,QS,C1,BGA947 | U2800,UB000 | CRITICAL | |

## Hall Effect AMR

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 677-10608 | 2 | HONEYWELL TRACK POWER, SOMC, INTERCONNECT, REFERENCE | J4800,J4801 | CRITICAL | |

## Power Controllers

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S01525 | 1 | IC,ISL92403HRZ-T,PWM,BUCK,WCSP40,0.4X3.3MM | U7000 | CRITICAL | |
| 338S00267 | 1 | IC,PMU,P6508339,7X7MM,BGA168 | U7800 | CRITICAL | |
| 353S01229 | 1 | IC,SUPPLY,INTERSIL,ISL6177AHRZ,TQFN,0.8P,4X4 | UA600 | CRITICAL | |
| 353S00928 | 1 | IC,ISL95208A,DRVR CPU REG,QFN44,EXPOSED | U7100 | CRITICAL | |

## Harpoon

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 339S00458 | 1 | IC,MODULE,MCU/DSP,MCHEPA,HARPOON,M,REV.7,QFN35 | U3730 | CRITICAL | |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 339S00428 | 339S00458 | | ALL | IC,MODULE,MCU/DSP,MCHEPA,HARPOON,M,REV.7,QFN35 |

## USB-C Connector

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 998-12556 | 2 | CONN,RECP,USB4,R-F,SC,R-A,3.0A,SMT | J3300,JB500 | CRITICAL | |

## Ocarina

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 338S00410 | 1 | IC,MEM,OCARINA,DS4SMX,079-AG,WCSP54 | U9000 | CRITICAL | |
| 338S00410 | 1 | IC,MEM,OCARINA,DS4SMX,079-AG,WCSP54 | U9500 | CRITICAL | OCARINA_2 |

## Programmable Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION | |
|---|---|---|---|---|---|---|
| 335S00199 | 1 | IC,SMBus SERIAL FLASH 32X32.4MM UTDFN8 PRO | UA701 | CRITICAL | CPUROM:BLANK | |
| 341S01017 | 1 | T29,TM1(V2.2),SEM-PROTO-2,SAFFORD | U2890 | CRITICAL | UPCROM_PROG:P1 | Updated-P1 |
| 341S01018 | 1 | T29,TM2(V2.1),SEM-PROTO-2,SAFFORD | UB090 | CRITICAL | UPCROM_PROG:P1 | Updated-P1 |
| 341S01025 | 1 | IC, BT ROM, EVT.VXX, SAFFORD | U3750 | CRITICAL | BT_ROM:P2 | Updated |
| 341S00725 | 1 | IC, WIFI ROM, PROTOX, SAFFORD | U3710 | CRITICAL | WIFI_ROM:P0 | Updated |

## H9M

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 339S00373 | 1 | DSP,GIGRALEXR+2GB 21NM,M,B0,NCK,CSP1406 | U3900 | CRITICAL | SOC:2GB |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 339S00373 | 339S00372 | | ALL | DSP,2GB,21NM,M,B0,NCK,CSP1406 |
| 339S00374 | 339S00373 | | ALL | DSP,2GB,21NM,M,B0,NCK,CSP1406 |
| 339S00371 | 339S00372 | | ALL | DSP,2GB,21NM,M,B0,NCK,CSP1406 |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 339S00376 | 1 | DSP,GIGRALEXR+1GB 21NM,M,B0,NCK,CSP1406 | U3900 | CRITICAL | SOC:1GB |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 339S00375 | 339S00376 | | ALL | DSP,1GB,21NM,M,B0,NCK,CSP1406 |
| 339S00372 | 339S00376 | | ALL | DSP,1GB,21NM,M,B0,NCK,CSP1406 |
| 339S00370 | 339S00376 | | ALL | DSP,1GB,21NM,M,B0,NCK,CSP1406 |

## S4E Parts

### 256GB

| | | | | | |
|---|---|---|---|---|---|
| 335S00324 | 4 | NAND,3D9,256GB,X2E,64L,1TR2,ED,TLC8110 | U9600,U9700,U9800,U9900 | CRITICAL | S4E_256_WD |
| 998-12418 | 4 | NAND,3D9,256GB,X2E,1TR2,T,KIOX,TLC8110 | U9600,U9700,U9800,U9900 | CRITICAL | S4E_256_TB |
| 998-12419 | 998-12418 | | ALL | SEM | |

### 512GB

| | | | | | |
|---|---|---|---|---|---|
| 335S00325 | 4 | NAND,3D9,128GB,X2E,64L,1TR2,ED,TLC8110 | U9600,U9700,U9800,U9900 | CRITICAL | S4E_512_WD |
| 998-12420 | 4 | NAND,3D9,128GB,X2E,1TR2,T,KIOX,TLC8110 | U9600,U9700,U9800,U9900 | CRITICAL | S4E_512_TB |
| 998-12421 | 998-12420 | | ALL | SEM | |

### 1TB

| | | | | | |
|---|---|---|---|---|---|
| 335S00326 | 6 | NAND,3D9,256GB,X2E,64L,1TR2,ED,TLC8110 | U9600,U9700,U9800,U9900,U9130,U9230 | CRITICAL | S4E_1TB_WD |
| 998-12422 | 6 | NAND,3D9,256GB,X2E,1TR2,T,KIOX,TLC8110 | U9600,U9700,U9800,U9900,U9130,U9230 | CRITICAL | S4E_1TB_TB |
| 998-12423 | 998-12422 | | ALL | SEM | |

### 2TB

| | | | | | |
|---|---|---|---|---|---|
| 335S00327 | 8 | NAND,3D9,256GB,X2E,64L,1TR2,ED,TLC8110 | [illegible] | CRITICAL | S4E_2TB_WD |
| 335S00321 | 8 | NAND,3D9,256GB,X2E,64L,2TR2,ED,TLC8110 | [illegible] | CRITICAL | S4E_2TB_SM |
| 998-12424 | 8 | NAND,3D9,256GB,X2E,1TR2,T,KIOX,TLC8110 | [illegible] | CRITICAL | S4E_2TB_TB |
| 998-12426 | 998-12424 | | ALL | SEM | |

### 4TB

| | | | | | |
|---|---|---|---|---|---|
| 335S00322 | 8 | NAND,3D9,512GB,X2E,2TR2,ED,TLC8110 | [illegible] | CRITICAL | S4E_4TB_SM |

### 2TB TLC

| | | | | | |
|---|---|---|---|---|---|
| 335S00228 | 8 | NAND,3D9,256GB,X2E,2TR2,T,TLC8110 | [illegible] | CRITICAL | TLC_2TB_TB |
| 335S00247 | 8 | NAND,3D9,256GB,X2E,2TR2,ED,TLC8110 | [illegible] | CRITICAL | TLC_2TB_WD |

FAB#:RC315

PAGE TITLE
BOM Configuration 2

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 3 OF 200
SHEET: 3 OF 131

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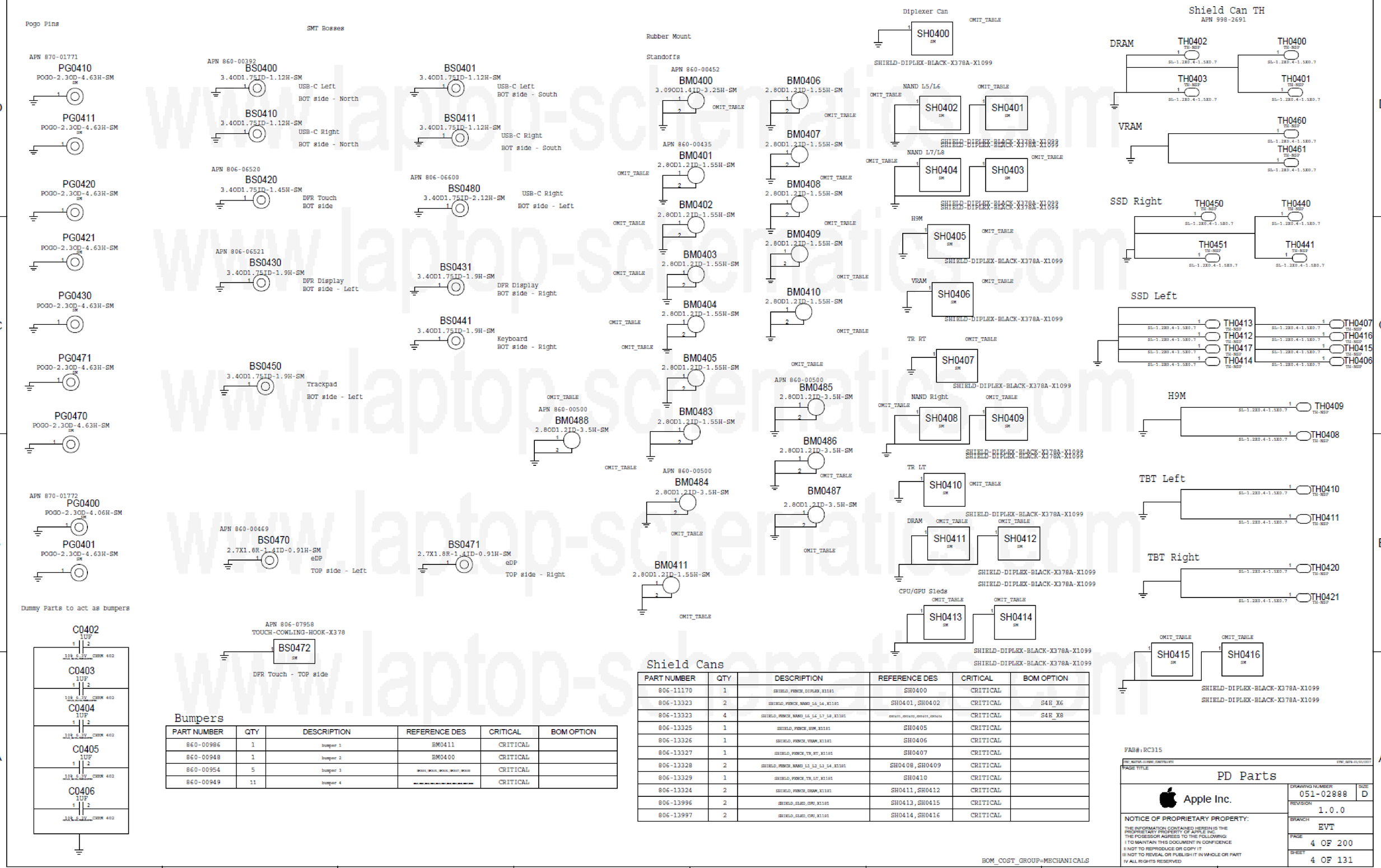


## Bumpers

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 860-00986 | 1 | bumper 1 | BM0411 | CRITICAL | |
| 860-00948 | 1 | bumper 2 | BM0400 | CRITICAL | |
| 860-00954 | 5 | bumper 3 | [illegible] | CRITICAL | |
| 860-00949 | 11 | bumper 4 | [illegible] | CRITICAL | |

## Shield Cans

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 806-11170 | 1 | SHIELD,FRENCH,DIPLEX,X1181 | SH0400 | CRITICAL | |
| 806-13323 | 2 | SHIELD,FRENCH,NAND_L5_L6,X1181 | SH0401,SH0402 | CRITICAL | S4E_X6 |
| 806-13323 | 4 | SHIELD,FRENCH,NAND_L5_L6_L7_L8,X1181 | SH0401,SH0402,SH0403,SH0404 | CRITICAL | S4E_X8 |
| 806-13325 | 1 | SHIELD,FRENCH,H9M,X1181 | SH0405 | CRITICAL | |
| 806-13326 | 1 | SHIELD,FRENCH,VRAM,X1181 | SH0406 | CRITICAL | |
| 806-13327 | 1 | SHIELD,FRENCH,TR,RT,X1181 | SH0407 | CRITICAL | |
| 806-13328 | 2 | SHIELD,FRENCH,NAND_L1_L2_L3_L4,X1181 | SH0408,SH0409 | CRITICAL | |
| 806-13329 | 1 | SHIELD,FRENCH,TR,LT,X1181 | SH0410 | CRITICAL | |
| 806-13324 | 2 | SHIELD,FRENCH,DRAM,X1181 | SH0411,SH0412 | CRITICAL | |
| 806-13996 | 2 | SHIELD,SLED,GPU,X1181 | SH0413,SH0415 | CRITICAL | |
| 806-13997 | 2 | SHIELD,SLED,CPU,X1181 | SH0414,SH0416 | CRITICAL | |

BOM_COST_GROUP=MECHANICALS

FAB#:RC315

PAGE TITLE
PD Parts

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REVISION 1.0.0
BRANCH EVT
PAGE 4 OF 200
SHEET 4 OF 131

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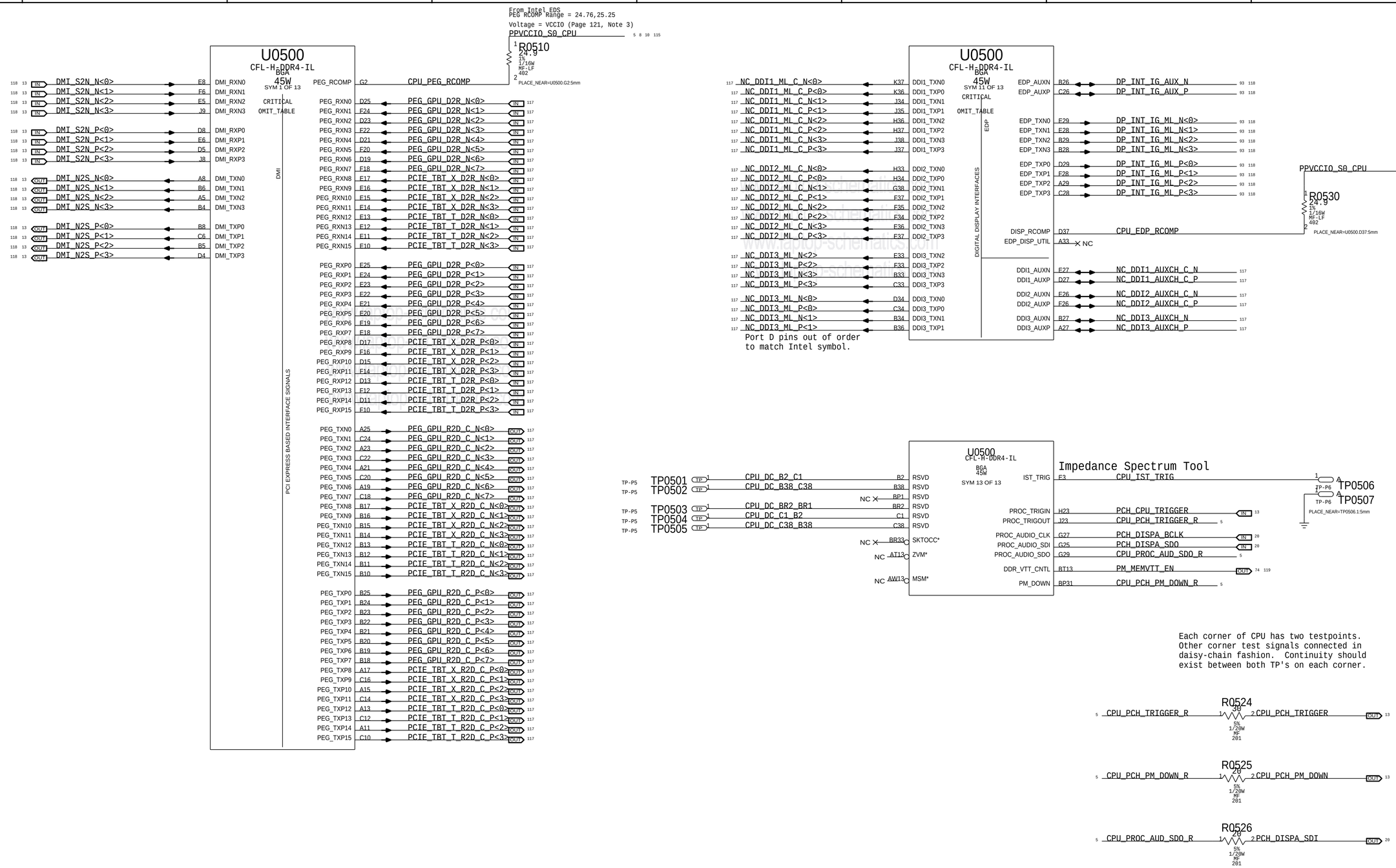


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

# CPU DMI/PEG/FDI/RSVD

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PAGE 5 OF 200

SHEET 5 OF 131

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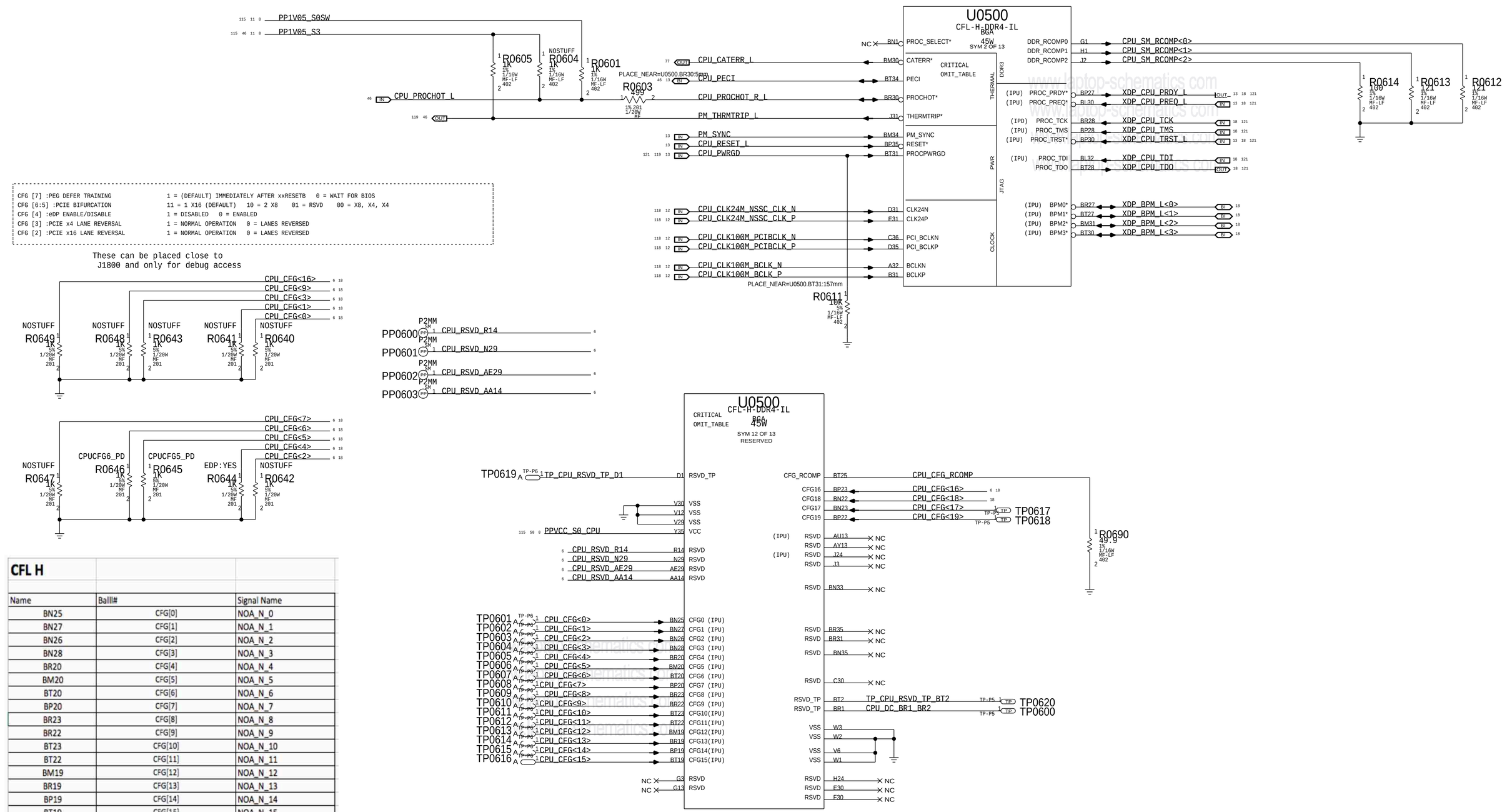


## CFL H

| Name | Ball# | Signal Name |
|---|---|---|
| BN25 | CFG[0] | NOA_N_0 |
| BN27 | CFG[1] | NOA_N_1 |
| BN26 | CFG[2] | NOA_N_2 |
| BN28 | CFG[3] | NOA_N_3 |
| BR20 | CFG[4] | NOA_N_4 |
| BM20 | CFG[5] | NOA_N_5 |
| BT20 | CFG[6] | NOA_N_6 |
| BP20 | CFG[7] | NOA_N_7 |
| BR23 | CFG[8] | NOA_N_8 |
| BR22 | CFG[9] | NOA_N_9 |
| BT23 | CFG[10] | NOA_N_10 |
| BT22 | CFG[11] | NOA_N_11 |
| BM19 | CFG[12] | NOA_N_12 |
| BR19 | CFG[13] | NOA_N_13 |
| BP19 | CFG[14] | NOA_N_14 |
| BT19 | CFG[15] | NOA_N_15 |
| | | |
| BN23 | CFG[17] | NOA_STB_P_0 |
| BP22 | CFG[19] | NOA_STB_P_1 |
| | | |
| D1 | RSVD_TP | PEG_VIEW0 |
| E1 | RSVD_TP | PEG_VIEW1 |
| E2 | RSVD_TP | PEG_VIEW3 |
| E3 | IST_TRIG | PEG_VIEW2 |
| BT2 | RSVD_TP | DDR_VIEW1 |
| BR1 | RSVD_TP | DDR_VIEW0 |

| BOM GROUP | BOM OPTIONS |
|---|---|
| CPUPEG:X8X8 | CPUCFG5_PD |
| CPUPEG:X8X4X4 | CPUCFG6_PD,CPUCFG5_PD |

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

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REVISION 1.0.0
BRANCH EVT
PAGE 6 OF 200
SHEET 6 OF 131

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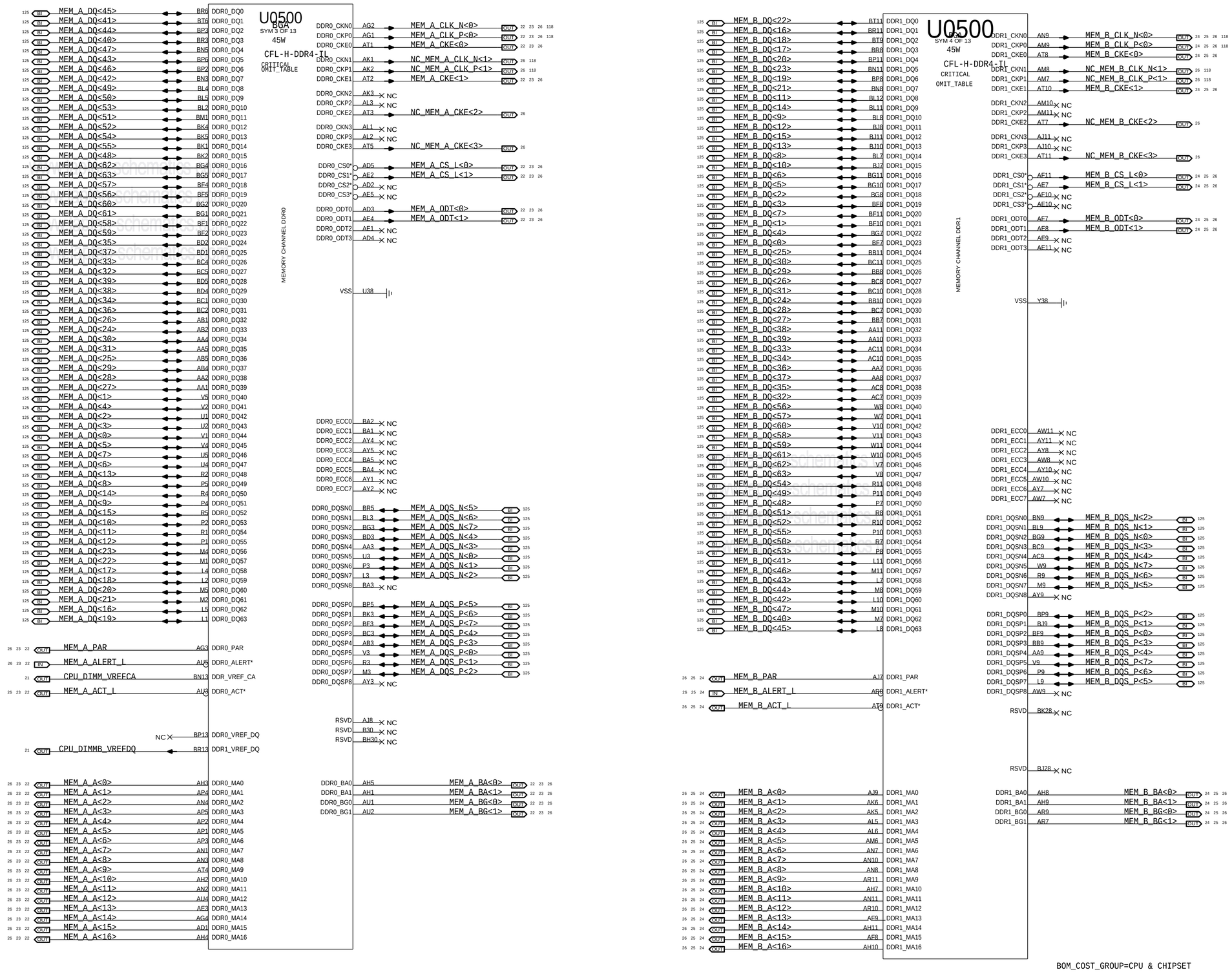


PAGE TITLE

# CPU DDR4 Interfaces

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PAGE 7 OF 200

SHEET 7 OF 131

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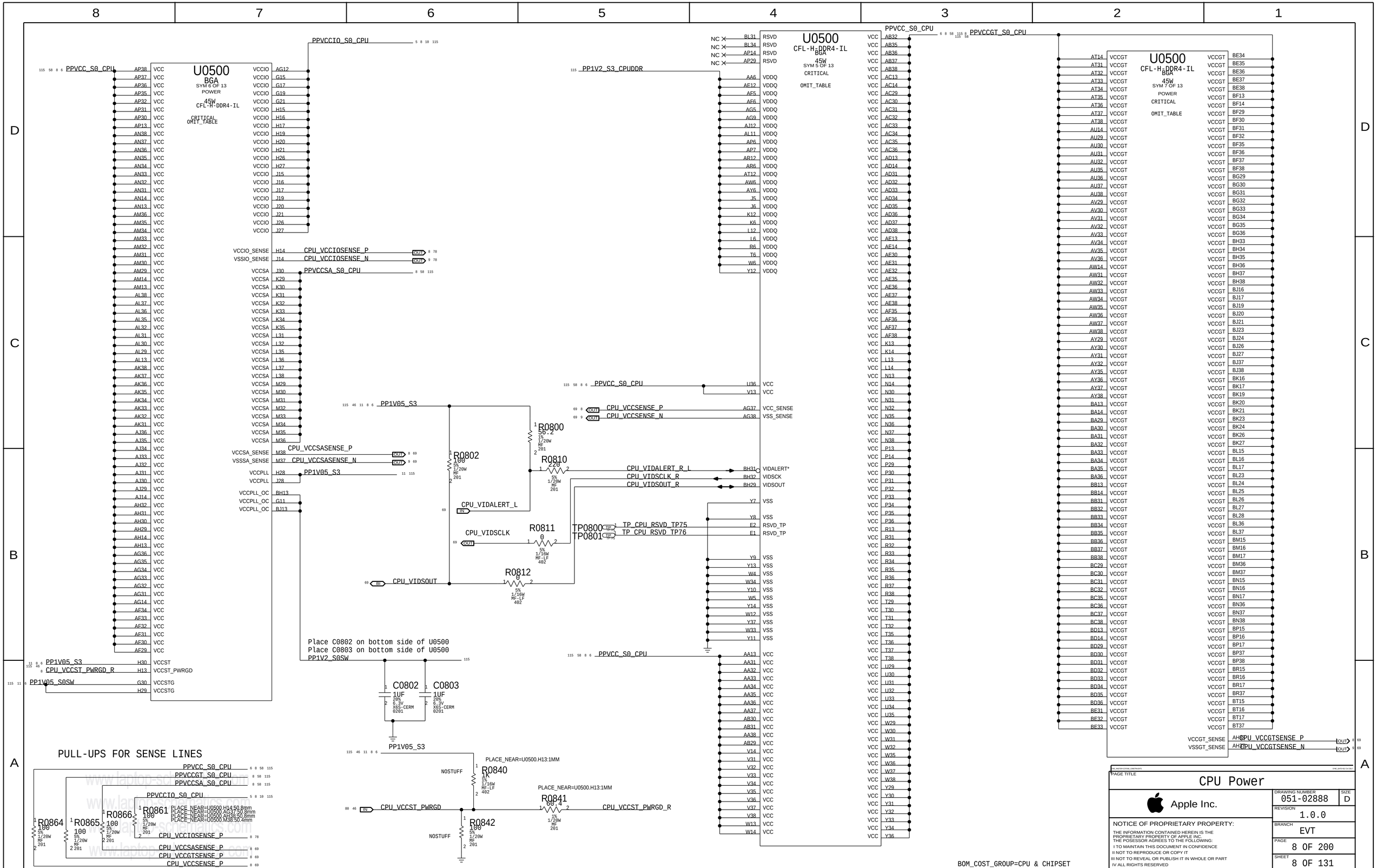
U0500
BGA
SYM 6 OF 13
POWER
45W
CFL-H-DDR4-IL
CRITICAL
OMIT_TABLE
U0500
CFL-H_DDR4-IL
BGA
45W
SYM 5 OF 13
CRITICAL
OMIT_TABLE
U0500
CFL-H_DDR4-IL
BGA
45W
SYM 7 OF 13
POWER
CRITICAL
OMIT_TABLE
PPVCCIO_S0_CPU
PPVCC_S0_CPU
PPVCCGT_S0_CPU
PPVCCSA_S0_CPU
PP1V2_S3_CPUDDR
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
PP1V05_S3
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
R0800 56.2
R0802 100
R0810 220
R0811 0
R0812 0
TP0800
TP0801
Place C0802 on bottom side of U0500
Place C0803 on bottom side of U0500
PP1V2_S0SW
C0802 1UF
C0803 1UF
PP1V05_S0SW
CPU_VCCST_PWRGD
CPU_VCCST_PWRGD_R
R0840 1K
R0841 60.4
R0842 100
PLACE_NEAR=U0500.H13:1MM
NOSTUFF
PULL-UPS FOR SENSE LINES
R0864 100
R0865 100
R0866 100
R0861 100
PLACE_NEAR=U0500.H14:50.8mm
PLACE_NEAR=U0500.AG37:50.8mm
PLACE_NEAR=U0500.AG38:50.8mm
PLACE_NEAR=U0500.M38:50.4mm
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU Power
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DRAWING NUMBER
051-02888
SIZE
D
REVISION
1.0.0
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PAGE
8 OF 200
SHEET
8 OF 131
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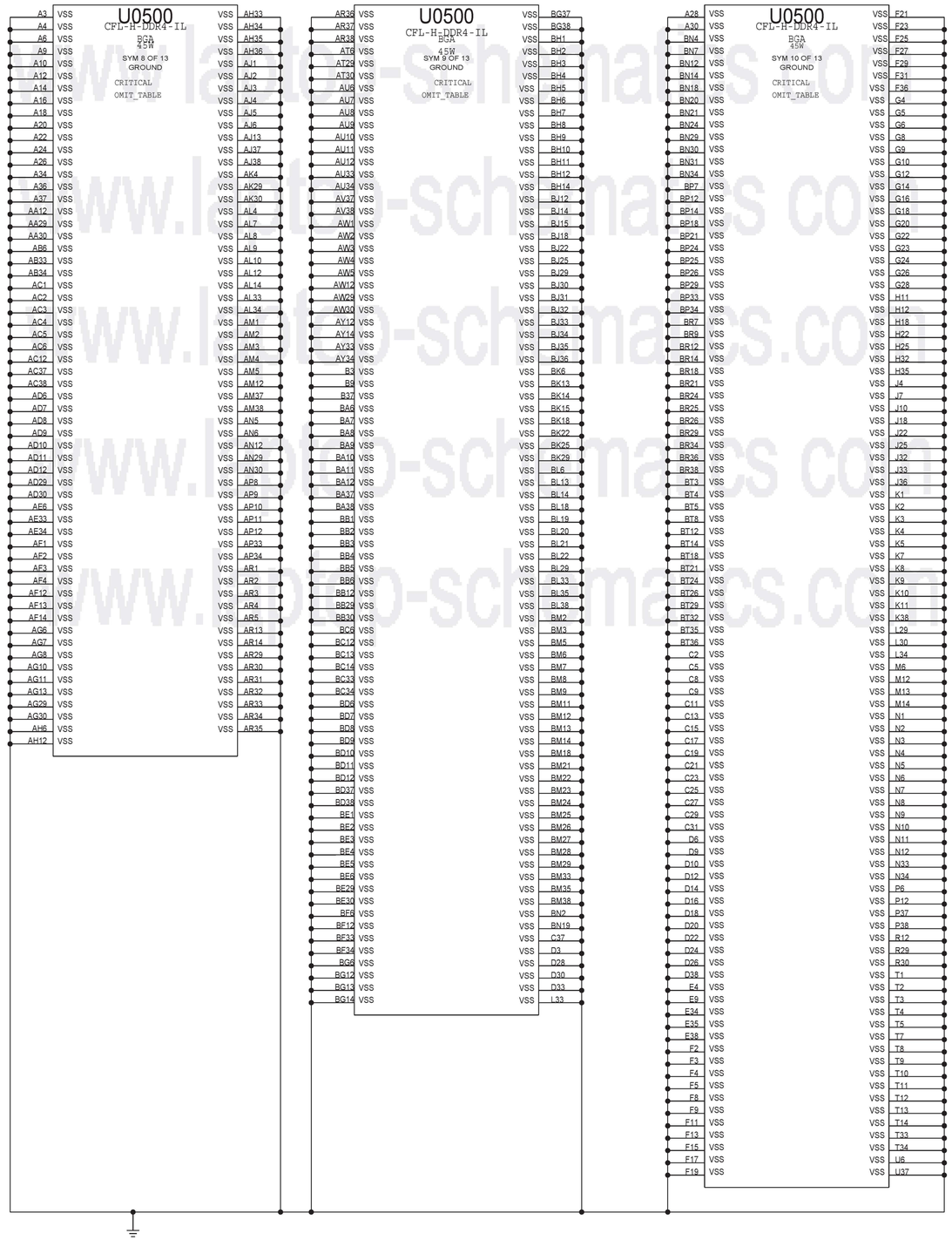


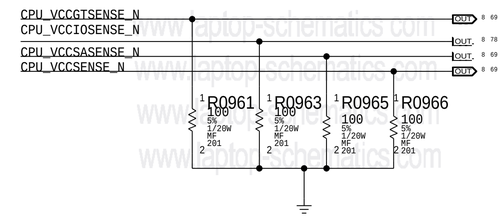


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SYNC_MASTER=J300_A19 SYNC_DATE=02/09/2017

PAGE TITLE

# CPU Ground

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PAGE 9 OF 200

SHEET 9 OF 131

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# Vcc CPU Core Decoupling from 20140905 BOM

## CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201  Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

115 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016 C1017 C1018 C1019 C1020 C1021 C1022
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 C1024 C1025 C1026 C1027 C1028 C1029 C1030 C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1038 C1039 C1040 C1041 C1042 C1043 C1044 C1045
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 C1047 C1048 C1049 C1050 C1051 C1052 C1053 C1054 C1055 C1056 C1057 C1058 C1059 C1060 C1061 C1062
1UF 20% 4V CERM-X6S 0201

Place near inductors on bottom side.

C10A0 C10A3 C10A4 C10Z4 C10A6 C10A7 C10A8 C10ZB C10B0 C10B1 C10B4 C10C0 C10C1 C10C4 C10C5 C10C6 C10C7
20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

C10D1 C10D2 C10D3 C10D4 C10D5 C10D6 C10E2 C10E3 C10N1 C10N2 C10N3 C10N4 C10N5 C10N6 C10N7
20UF 20% 2.5V X6S-CERM 0402-1; 12PF 5% 25V NP0-C0G 0201

C10F0 C10F1 C10F2 C10F3 C10F4 C10F5 C10F6 C10F7 C10F8 C10F9 C10G0
20UF 20% 2.5V X6S-CERM 0402-1

C1068 C1069 C1070 C1072 C1073
220UF 20% 2V ELEC SM-COMBO

122 115 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 C1081 C1082 C1083 C1084 C1085
20UF 20% 2.5V X6S-CERM 0402-1

Place on bottom side of U0500

C1090 C1091 C1092 C1093 C1094 C1095 C1096
20UF 20% 2.5V X6S-CERM 0402-1; 220UF 20% 2V ELEC SM-COMBO

## CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

## CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

Place near U0500 on bottom side

115 8 5 PPVCCIO_S0_CPU

C1086 C1087 C1088 C1089 C108A C108B C108C C108D
20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Decoupling 1

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DRAWING NUMBER: 051-02888  SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 10 OF 200
SHEET: 10 OF 131

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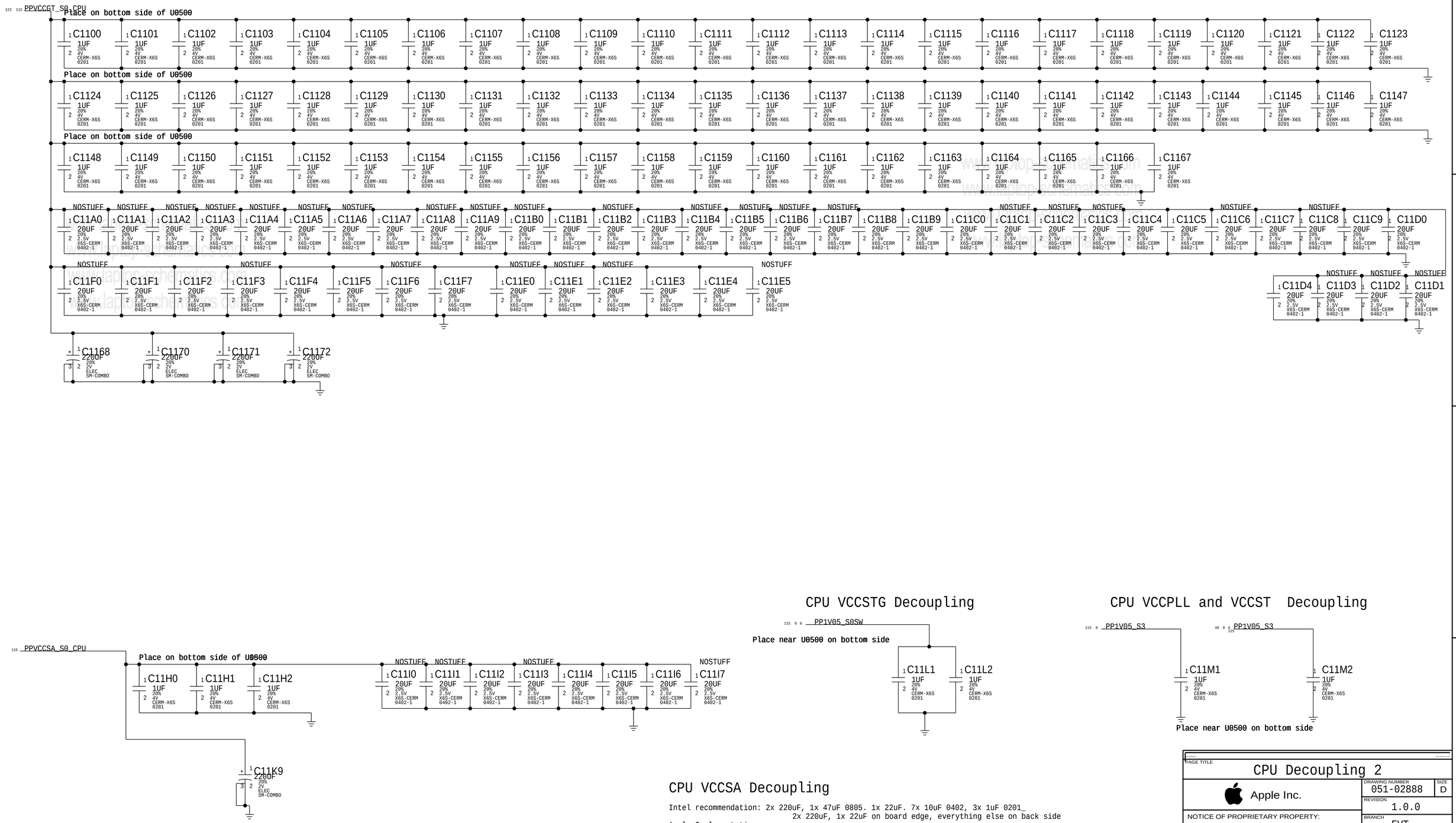
# Vcc GT Slice Core Decoupling from 20140905 BOM

## CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side




## CPU VCCSTG Decoupling




## CPU VCCPLL and VCCST Decoupling







## CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU Decoupling 2

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DRAWING NUMBER 051-02888 SIZE D
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PAGE 11 OF 200
SHEET 11 OF 131

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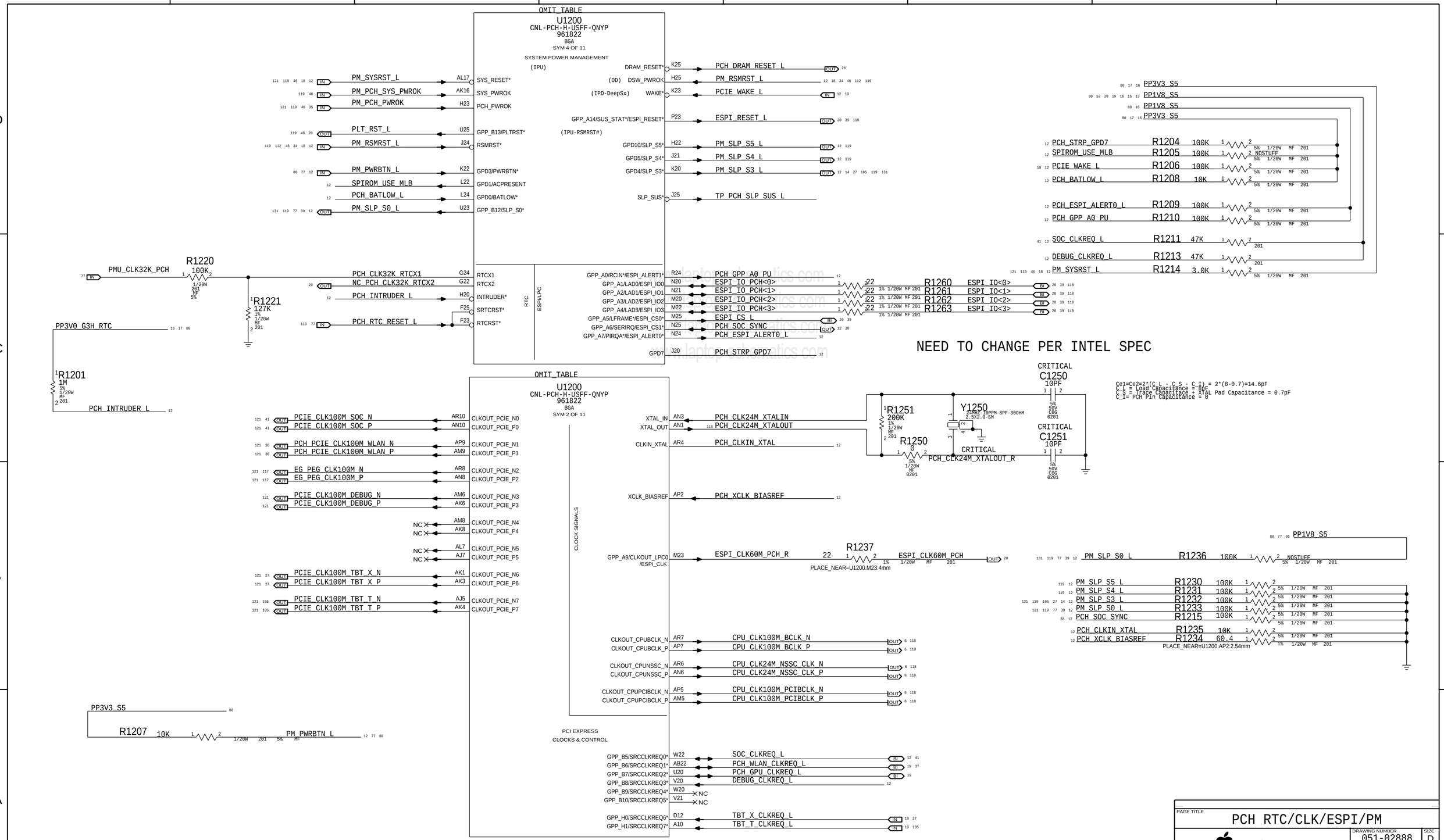


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PAGE TITLE
# PCH RTC/CLK/ESPI/PM

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SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 12 OF 200
SHEET 12 OF 131

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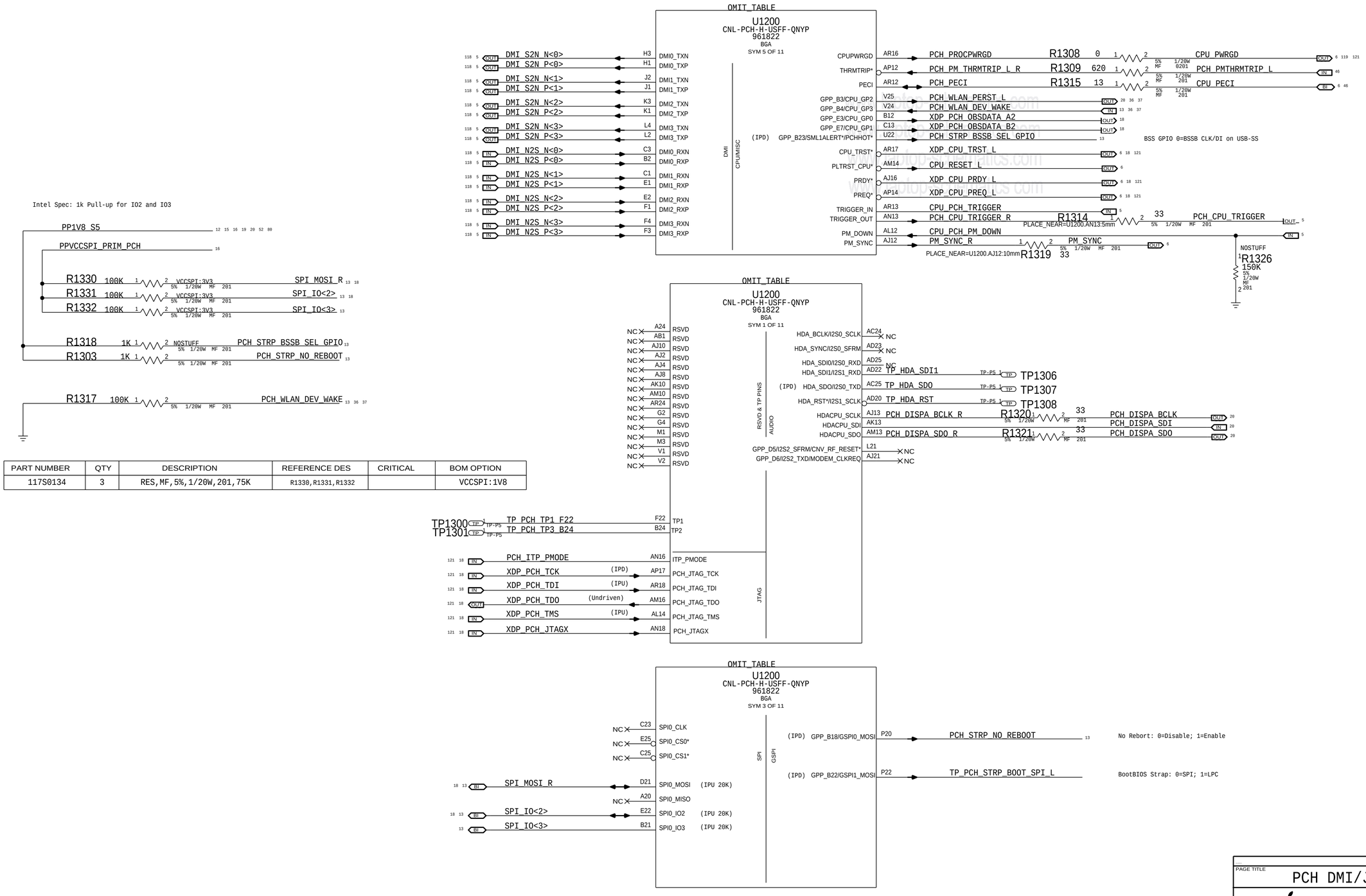


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0134 | 3 | RES,MF,5%,1/20W,201,75K | R1330,R1331,R1332 | | VCCSPI:1V8 |

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
# PCH DMI/JTAG/SPI/HDA

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BRANCH EVT
PAGE 13 OF 200
SHEET 13 OF 131

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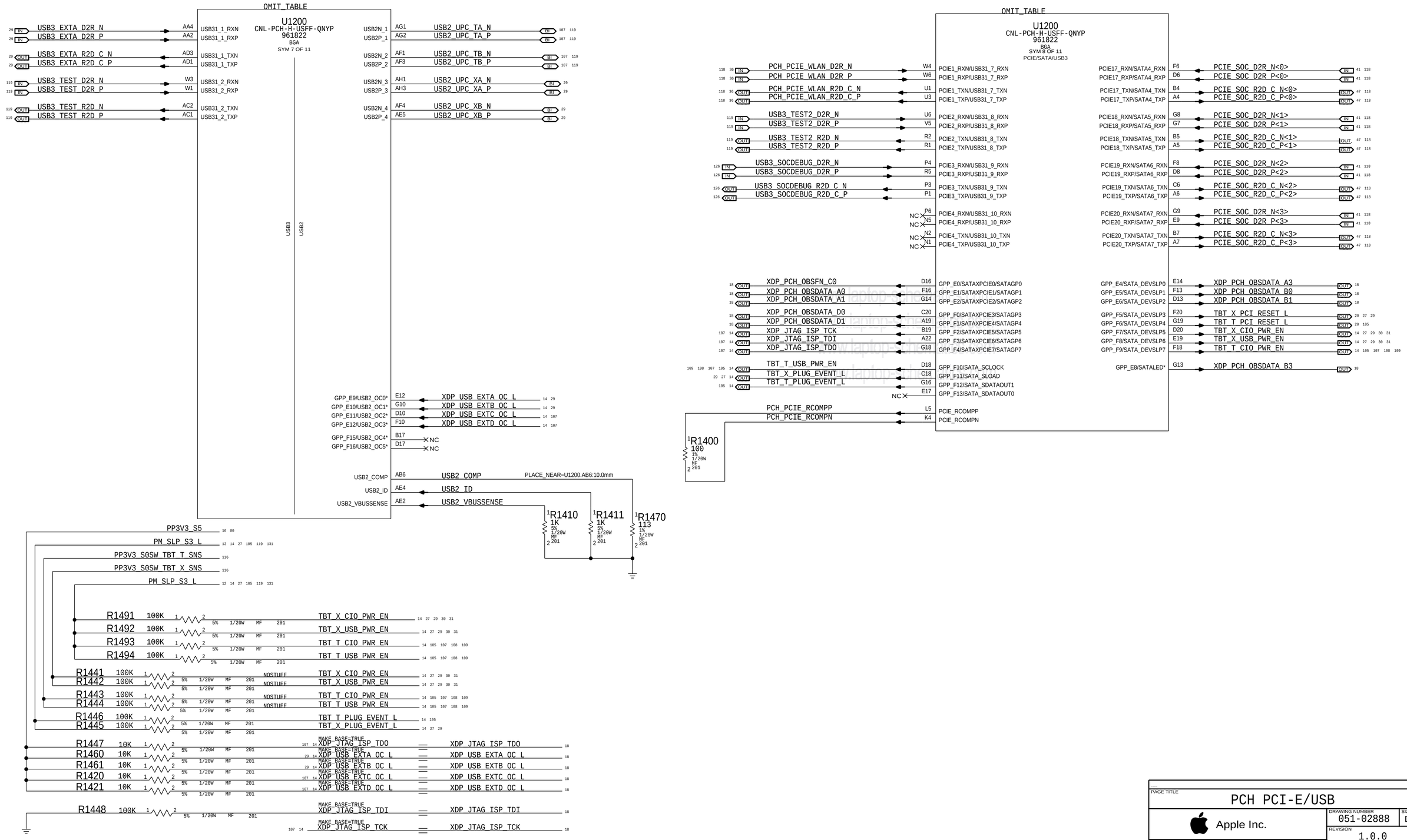


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH PCI-E/USB

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DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 14 OF 200
SHEET 14 OF 131

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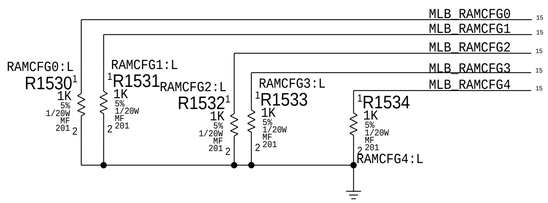
| SPEED | CONGIF3 |
|---|---|
| 2400MHZ | 0 |
| 2133MHZ | 1 |

| STORAGE | CONGIF2 |
|---|---|
| 16GB | 1 |
| 32GB | 0 |

| VENDOR | CONGIF1 | CONGIF0 |
|---|---|---|
| SAMSUNG | 1 | 0 |
| MICRON | 0 | 1 |
| HYNIX | 0 | 0 |




OMIT_TABLE

U1200
CNL-PCH-H-USFF-QNYP
961822
BGA
SYM 9 OF 11

| | | | | |
|---|---|---|---|---|
| | | A18 | GPP_F14/PS_ON* | NC |
| 93 15 OUT | EDP_IG PANEL PWR | A16 | GPP_F19/EDP_VDDEN | |
| 93 15 OUT | EDP_IG BKLT_EN | C16 | GPP_F20/EDP_BKLTEN | |
| | | A14 | GPP_F21/EDP_BKLTCTL | NC |
| | | B14 | GPP_F22/DDPF_CTRLCLK | NC |
| | | A13 | GPP_F23/DDPF_CTRLDATA | NC |
| | | AN23 | GPP_I0/DDPB_HPD0/DISP_MISC0 | NC |
| | | AN25 | GPP_I1/DDPC_HPD1/DISP_MISC1 | NC |
| | | AP24 | GPP_I2/DDPD_HPD2_DISP_MISC2 | NC |
| | | AP22 | GPP_I3/DDPF_HPD3_DISP_MISC3 | NC |
| 93 15 IN | DP_INT_IG_HPD | AR22 | GPP_I4/EDP_HPD/DISP_MISC4 | |
| | | AP19 | GPP_I5/DDPB_CTRLCLK | NC |
| | | AM19 | GPP_I6/DDPB_CTRLDATA | NC |
| | | AR20 | GPP_I7/DDPC_CTRLCLK | NC |
| | | AN20 | GPP_I8/DDPC_CTRLDATA | NC |
| | | AP21 | GPP_I9/DDPD_CTRLCLK | NC |
| | | AR21 | GPP_I10/DDPD_CTRLDATA | NC |
| | | AL24 | GPP_I11/M2_SKT2_CFG0 | NC |
| | | AL25 | GPP_I12/M2_SKT2_CFG1 | NC |
| 107 29 15 OUT | TBT_POC_RESET | AK25 | GPP_I13/M2_SKT2_CFG2 | |
| 15 | PCH_STRP_SPIROM_SAF | A9 | GPP_H12/SML2ALERT* (IPD) | |
| 15 | PCH_STRP_GPP_H15 | B9 | GPP_H15/SML3ALERT* | |
| 19 15 IN | WLAN_AUDIO_SYNC_LS3V3 | C10 | GPP_H23/TIME_SYNC0 | |

GPPF/ BACKLIGHT
GPPI/DISPLAY
GPPG
GPPH/I2C/INTEGRATED SENSOR /SMLINK

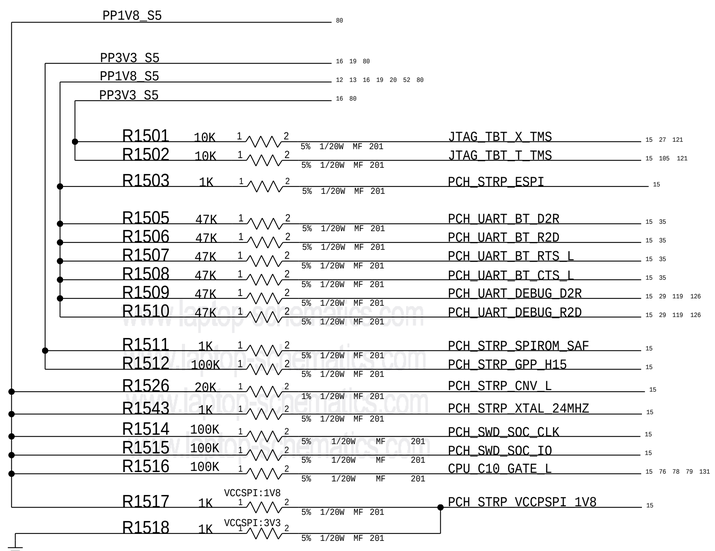
J680 Display Port DDPF Disabled

PDG recommends to NC the HPD lines not being used

J680 Display Port DDPB/C/D Disabled

eSPI Flash Mode: 0=MAF; 1=SAF

| | | | | |
|---|---|---|---|---|
| | | AM18 | GPP_J0/CNV_PA_BLANKING | SOC_SWD_MUX_SEL_PCH 15 |
| | | AK18 | GPP_J1/CPU_C10_GATE* | CPU_C10_GATE_L OUT 15 76 78 79 131 |
| | | AL19 | GPP_J2 | PCH_SWD_SOC_CLK 15 GPP_J2:Unused |
| | | AJ18 | GPP_J3 | PCH_SWD_SOC_IO 15 GPP_J3:Unused |
| | (IPD) | AJ22 | GPP_J4/CNV_BRI_DT/UART0B_RTS* | PCH_STRP_XTAL_24MHZ 15 GPP_J4: 0=38.4MHz 1=24MHz XTAL |
| | | AH23 | GPP_J5/CNV_BRI_RSP/UART0B_RXD | MLB_RAMCFG2 15 |
| | | AJ25 | GPP_J6/CNV_RGI_DT/UART0B_TXD | PCH_STRP_CNV_L 15 GPP_J6: 0=ENABLE 1=DISABLE |
| | | AH25 | GPP_J7/CNV_RGI_RSP/UART0B_CTS* | MLB_RAMCFG3 15 |
| | | AK22 | GPP_J8/CNV_MFUART2_RXD | MLB_RAMCFG4 15 |
| | | AK23 | GPP_J9/CNV_MFUART2_TXD | PCH_STRP_VCCPSPI_1V8 15 GPP_J9: 0=3.3V; 1=1.8V |
| | (IPD) | AM20 | GPP_J10 | PCH_BT_ROM_BOOT_L 15 36 |
| | | AK20 | GPP_J11/A4WP_PRESENT | PCH_BT_DEV_WAKE 15 36 |
| | | A8 | GPP_K20 | MLB_RAMCFG0 15 |
| | | C8 | GPP_K21 | MLB_RAMCFG1 15 |
| | | AJ17 | GPPJ_RCOMP_1P8 | PCH_GPPJ_RCOMP_1P8 15 |
| | | AG24 | CNV_WR_CLKP | NC |
| | | AG25 | CNV_WR_CLKN | NC |
| | | AF23 | CNV_WR_D0P | NC |
| | | AF25 | CNV_WR_D0N | NC |
| | | AE22 | CNV_WR_D1P | NC |
| | | AE24 | CNV_WR_D1N | NC |
| | | AH22 | CNV_WT_CLKP | NC |
| | | AH20 | CNV_WT_CLKN | NC |
| | | AG21 | CNV_WT_D0P | NC |
| | | AG20 | CNV_WT_D0N | NC |
| | | AF22 | CNV_WT_D1P | NC |
| | | AF20 | CNV_WT_D1N | NC |
| | | AE21 | CNV_WT_RCOMP | NC |



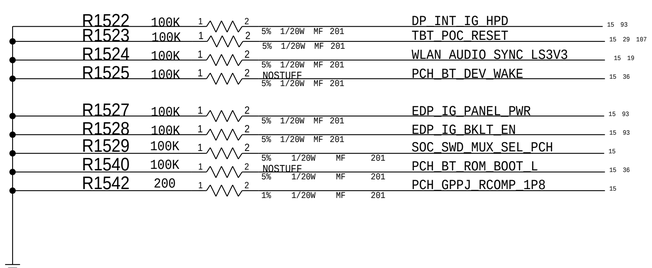

OMIT_TABLE

U1200
CNL-PCH-H-USFF-QNYP
961822
BGA
SYM 6 OF 11

| | | | | |
|---|---|---|---|---|
| 39 20 OUT | SOC_PERST_L | R22 | GPP_A20/ISH_GP2 | |
| 39 IN | PCH_GCON_INT_L | P25 | GPP_A21/ISH_GP3 | |
| TP1501 TP TP-P5 PLACE_SIDE=BOTTOM | TP_PCH_STRP_TOPBLK_SWP_L | R21 | GPP_B14/SPKR (IPD) | |
| 121 27 15 OUT | JTAG_TBT_X_TMS | AC20 | GPP_D0/SPI1_CS*/SBK0/BK0 | |
| 121 105 15 OUT | JTAG_TBT_T_TMS | AC21 | GPP_D1/SPI1_CLK/SBK1/BK1 | |
| | | AB20 | GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI | NC |

GPPA/ INTEGRATED SENSOR
GPPB
GPPD/INTEGRATED SENSOR/UART/I2C
GPPC/SMLINK/I2C/UART

| | | | | |
|---|---|---|---|---|
| | | W23 | GPP_C0/SMBCLK | SMBUS_PCH_CLK OUT 52 |
| | | W25 | GPP_C1/SMBDATA | SMBUS_PCH_DATA BI 52 PROJ-SPECIFIC PULLUP |
| | (IPD) | AA22 | GPP_C2/SMBALERT* | TP_PCH_STRP_TLSCONF TLS: 0=Disbale; 1=Enable |
| | (IPD) | AB19 | GPP_C5/SML0ALERT* | PCH_STRP_ESPI 15 GPP_C5: 0=LPC; 1=eSPI |
| | | AA24 | GPP_C8/UART0A_RXD | PCH_UART_BT_D2R IN 15 35 |
| | | AA21 | GPP_C9/UART0A_TXD | PCH_UART_BT_R2D OUT 15 35 |
| | | AA18 | GPP_C10/UART0A_RTS* | PCH_UART_BT_RTS_L OUT 15 35 |
| | | Y19 | GPP_C11/UART0A_CTS* | PCH_UART_BT_CTS_L IN 15 35 |
| | | AB25 | GPP_C20/UART2_RXD | PCH_UART_DEBUG_D2R IN 15 29 119 126 |
| | | AB23 | GPP_C21/UART2_TXD | PCH_UART_DEBUG_R2D OUT 15 29 119 126 |

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PAGE TITLE
PCH GPIO/MISC/NCTF

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SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 15 OF 200
SHEET 15 OF 131

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OMIT_TABLE

U1200
CNL-PCH-H-USFF-QNYP
961822
BGA
SYM 10 OF 11
POWER

| Signal | Pin | Net / Notes |
|---|---|---|
| PRIMARY WELL | | |
| 115 80 17 PP1V05_PRIM | AB12 | VCCPRIM_1P05 |
| | AB14 | VCCPRIM_1P05 |
| | AB17 | VCCPRIM_1P05 |
| | AB7 | VCCPRIM_1P05 |
| | AB9 | VCCPRIM_1P05 |
| | AD12 | VCCPRIM_1P05 |
| | AD14 | VCCPRIM_1P05 |
| | AD9 | VCCPRIM_1P05 |
| | AE11 | VCCPRIM_1P05 |
| | AF7 | VCCPRIM_1P05 |
| | H7 | VCCPRIM_1P05 |
| | H9 | VCCPRIM_1P05 |
| | J15 | VCCPRIM_1P05 |
| | K14 | VCCPRIM_1P05 |
| | K17 | VCCPRIM_1P05 |
| | K7 | VCCPRIM_1P05 |
| | K9 | VCCPRIM_1P05 |
| | M7 | VCCPRIM_1P05 |
| | M9 | VCCPRIM_1P05 |
| | P12 | VCCPRIM_1P05 |
| | P14 | VCCPRIM_1P05 |
| | P17 | VCCPRIM_1P05 |
| | P7 | VCCPRIM_1P05 |
| | P9 | VCCPRIM_1P05 |
| | T12 | VCCPRIM_1P05 |
| | T14 | VCCPRIM_1P05 |
| | T17 | VCCPRIM_1P05 |
| | T7 | VCCPRIM_1P05 |
| | T9 | VCCPRIM_1P05 |
| | V12 | VCCPRIM_1P05 |
| | V14 | VCCPRIM_1P05 |
| | V17 | VCCPRIM_1P05 |
| | V9 | VCCPRIM_1P05 |
| | Y12 | VCCPRIM_1P05 |
| | Y14 | VCCPRIM_1P05 |
| | Y17 | VCCPRIM_1P05 |
| | Y7 | VCCPRIM_1P05 |
| | Y9 | VCCPRIM_1P05 |
| PRIMARY WELL HVCMOS | | |
| 80 17 12 PP3V3_S5 | AD17 | VCCPRIM_3P3 |
| | AE15 | VCCPRIM_3P3 |
| | AE18 | VCCPRIM_3P3 |
| | M17 | VCCPRIM_3P3 |
| | V7 | VCCPRIM_3P3 |
| 17 PP1V05_PRIM_PCH_VCCAPLL_F | AF6 | VCCAPLL_1P05 |
| | AG8 | VCCAPLL_1P05 |
| 115 PP1V05_PRIM | AC5 | VCCDUSB_1P05 |
| 115 PP1V05_PRIM | AJ6 | VCCA_BCLK_1P05 |
| 115 PP1V05_PRIM | AG5 | VCCA_SRC_1P05 |
| 17 PP1V05_PRIM_PCH_VCCAXTAL_F | AD7 | VCCA_XTAL_1P05 |
| 80 17 PP1V8_S5 Share with GPIO J Group Power | AG11 | VCCPRIM_1P8 |
| | AG13 | VCCPRIM_1P8 |
| | AH12 | VCCPRIM_1P8 |
| | AH14 | VCCPRIM_1P8 |
| 115 17 PP1V05_PRIM | K6 | VCCPRIM_MPHY_1P05 |
| HD AUDIO POWER | | |
| 17 PP1V8_S0_PCH_VCCHDA_F | AD19 | VCCHDA |

| Signal | Pin | Net / Notes |
|---|---|---|
| AUDIO PLL | | |
| MOD PHY PRIMARY | | |
| VCCDPHY_1P24 | AF19 | PP1V24_S5_PCH_VCCDPHY 17 |
| VCCDPHY_1P24 | AG18 | |
| VCCDPHY_1P24 | AH17 | |
| VCCDPHY_1P24 | AH19 | |
| VCCDSW_3P3 | M19 | PP3V3_S5 12 17 80 |
| VCCDSW_1P05 | N18 | PP1V05_S5_PCH_VCCDSW 17 Internal Supply |
| DEEP SX WELL | | |
| VCCAMPHYPLL_1P05 | M6 | PP1V_PRIM_PCH_VCCAMPHYPLL_F 17 |
| LDO | | |
| VCCPHVLDO_1P8 | AF12 | |
| VCCPHVLDO_1P8 | AF14 | PP1V8_PCH_VCCPHYLDO 17 Internal LDO, leave this pin as NC |
| GPPA PRIMARY WELL | | |
| VCCPGPPA | P19 | PP1V8_S5 12 80 |
| GPPB/GPPC PRIMARY WELL | | |
| VCCPGPPBC | T19 | PP1V8_S5 12 13 15 19 20 52 80 |
| GPPD PRIMARY WELL | | |
| VCCPGPPD | V19 | PP3V3_S5 15 80 |
| GPPE/GPPEF PRIMARY WELL | | |
| VCCPGPPEF | M12 | PP3V3_S5 14 80 |
| VCCPGPPEF | M14 | |
| GPPH/GPPK PRIMARY WELL | | |
| VCCPGPPHK | K12 | PP3V3_S5 15 19 80 |
| DCPRTC | H17 | PPDCPRTC_PCH 17 |
| RTC WELL SUPPLY | | |
| VCCRTC | G20 | PP3V0_G3H_RTC 12 17 80 |
| VCCRTC | H19 | |
| RTC LOGIC PW/VRM | | |
| SPI | | |
| VCCSPI | K19 | PPVCCSPI_PRIM_PCH |
| ANALOG PLL USB2/VRM | | |

VOLTAGE=3.3V
R1601 0 0201 MF 1/20W 5% VCCSPI:3V3
PP3V3_S5 80

R1602 0 0201 MF 1/20W 5% VCCSPI:1V8
PP1V8_S5 80

OMIT_TABLE

U1200
CNL-PCH-H-USFF-QNYP
961822
BGA
SYM 11 OF 11

| Pin | Net |
|---|---|
| R6 | VSS |
| U13 | VSS |
| A12 | VSS |
| A1 | VSS |
| A2 | VSS |
| AJ24 | VSS |
| AP4 | VSS |
| D5 | VSS |
| G17 | VSS |
| J11 | VSS |
| L20 | VSS |
| AL1 | VSS |
| AA20 | VSS |
| AC22 | VSS |
| AG4 | VSS |
| AH9 | VSS |
| AJ1 | VSS |
| AJ9 | VSS |
| AJ14 | VSS |
| AJ19 | VSS |
| AJ20 | VSS |
| AL2 | VSS |
| AR14 | VSS |
| AR19 | VSS |
| AL4 | VSS |
| AL9 | VSS |
| AL22 | VSS |
| AM7 | VSS |
| AM12 | VSS |
| AM17 | VSS |
| AM21 | VSS |
| AP1 | VSS |
| AP25 | VSS |
| AR1 | VSS |
| AR2 | VSS |
| AR5 | VSS |
| AR9 | VSS |
| E24 | VSS |
| G1 | VSS |
| AR25 | VSS |
| B1 | VSS |
| B25 | VSS |
| D7 | VSS |
| D9 | VSS |
| D14 | VSS |
| D19 | VSS |
| E4 | VSS |
| E7 | VSS |
| J5 | VSS |
| J8 | VSS |
| G5 | VSS |
| G12 | VSS |
| G21 | VSS |
| G25 | VSS |
| H4 | VSS |
| H6 | VSS |
| H12 | VSS |
| H14 | VSS |
| J4 | VSS |
| J6 | VSS |
| J13 | VSS |
| J22 | VSS |
| J18 | VSS |
| N15 | VSS |
| R4 | VSS |
| R8 | VSS |
| L1 | VSS |
| L6 | VSS |
| L8 | VSS |
| L11 | VSS |
| L13 | VSS |
| L15 | VSS |
| L18 | VSS |
| L25 | VSS |
| M4 | VSS |
| N4 | VSS |
| N6 | VSS |
| N8 | VSS |
| N11 | VSS |
| N13 | VSS |
| N22 | VSS |
| U4 | VSS |
| U8 | VSS |
| R11 | VSS |
| R13 | VSS |
| R15 | VSS |
| R18 | VSS |
| R20 | VSS |
| R25 | VSS |
| U15 | VSS |
| U11 | VSS |
| W13 | VSS |
| W18 | VSS |
| U18 | VSS |
| V4 | VSS |
| V6 | VSS |
| V22 | VSS |
| W8 | VSS |
| W11 | VSS |
| W15 | VSS |
| A25 | VSS |
| AA1 | VSS |
| AA5 | VSS |
| A17 | VSS |
| A21 | VSS |
| AA25 | VSS |
| AB3 | VSS |
| AA6 | VSS |
| AA8 | VSS |
| AA11 | VSS |
| AA13 | VSS |
| AA15 | VSS |
| AC4 | VSS |
| AC6 | VSS |
| AB4 | VSS |
| AC8 | VSS |
| AE1 | VSS |
| AE6 | VSS |
| AE8 | VSS |
| AE13 | VSS |
| AC11 | VSS |
| AC13 | VSS |
| AC15 | VSS |
| AC18 | VSS |
| AD4 | VSS |
| AD6 | VSS |
| AE20 | VSS |
| AE25 | VSS |
| AF9 | VSS |
| AF17 | VSS |
| AG6 | VSS |
| AG15 | VSS |
| AG22 | VSS |
| AH4 | VSS |
| AH6 | VSS |
| AH7 | VSS |
| B22 | VSS |

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

www.laptop-schematics.com

PAGE TITLE: PCH Power

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REVISION: 1.0.0

BRANCH: EVT

PAGE: 16 OF 200

SHEET: 16 OF 131

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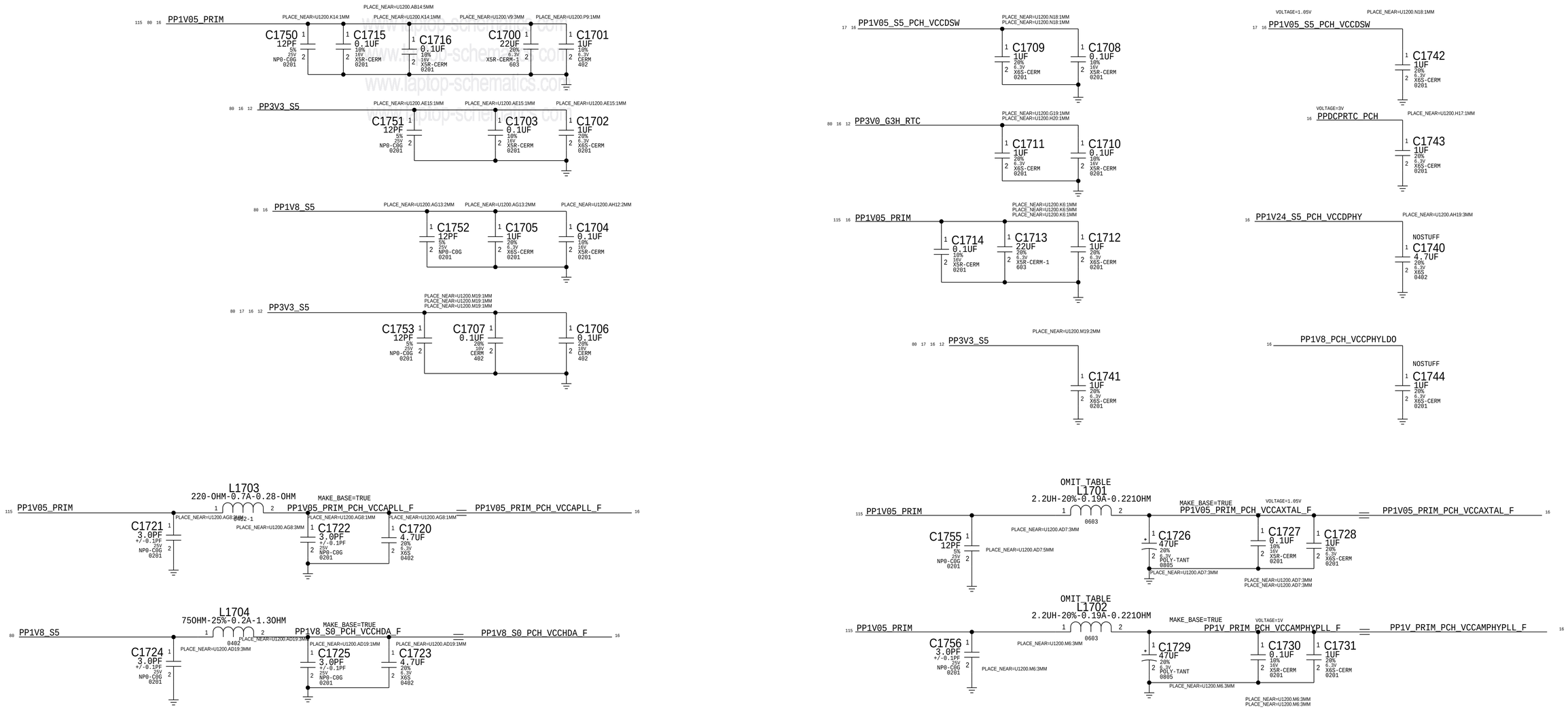


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 113S0022 | 2 | RES,MF,1A MAX,00HM,5%,0603 | L1701,L1702 | | |

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Decoupling

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 17 OF 200
SHEET 17 OF 131

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## Extra BPM Testpoints

XDP_BPM_L<0> — TP1800
XDP_BPM_L<1> — TP1801
XDP_BPM_L<2> — TP1802
XDP_BPM_L<3> — TP1803

## Primary / Merged (CPU/PCH) Micro2-XDP

PP1V05_PRIM

PULL CFG<3> LOW WHEN XDP PRESENT
R1801 1.5K 5% 1/20W MF 201 — XDP:YES NO_XNET_CONNECTION
PLACE_NEAR=J1800.2:5MM

XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| XDP_PRESENT_CPU | | | XDP_PIN_1 |
| XDP_CPU_PREQ_L | OBSFN_A0 | | |
| XDP_CPU_PRDY_L | OBSFN_A1 | | |
| CPU_CFG<0> | OBSDATA_A0 | | |
| CPU_CFG<1> | OBSDATA_A1 | | |
| CPU_CFG<2> | OBSDATA_A2 | | |
| CPU_CFG<3> | OBSDATA_A3 | | |
| NC | OBSFN_B0 | | |
| NC | OBSFN_B1 | | |
| CPU_CFG<4> | OBSDATA_B0 | | |
| CPU_CFG<5> | OBSDATA_B1 | | |
| CPU_CFG<6> | OBSDATA_B2 | | |
| CPU_CFG<7> | OBSDATA_B3 | | |
| XDP_PM_RSMRST_L | HOOK0 | | |
| XDP_CPU_PWRBTN_L | HOOK1 | | |
| | VCC_OBS_AB | | |
| NC | HOOK2 | | |
| SPI_MOSI_R_CONN | HOOK3 | | |
| NC | SDA | | |
| NC | SCL | | |
| XDP_PCH_TCK | TCK1 | | |
| | TCK0 | | |
| | | | XDP_PRESENT# |
| | | OBSFN_C0 | CPU_CFG<17> |
| | | OBSFN_C1 | CPU_CFG<16> |
| | | OBSDATA_C0 | CPU_CFG<8> |
| | | OBSDATA_C1 | CPU_CFG<9> |
| | | OBSDATA_C2 | CPU_CFG<10> |
| | | OBSDATA_C3 | CPU_CFG<11> |
| | | OBSFN_D0 | CPU_CFG<19> |
| | | OBSFN_D1 | CPU_CFG<18> |
| | | OBSDATA_D0 | CPU_CFG<12> |
| | | OBSDATA_D1 | CPU_CFG<13> |
| | | OBSDATA_D2 | CPU_CFG<14> |
| | | OBSDATA_D3 | CPU_CFG<15> |
| | | ITPCLK/HOOK4 | NC_ITPXDP_CLK100MP |
| | | ITPCLK#/HOOK5 | NC_ITPXDP_CLK100MN |
| | | VCC_OBS_CD | |
| | | RESET#/HOOK6 | PCH_ITP_PMODE |
| | | DBR#/HOOK7 | XDP_DBRESET_L |
| | | TDO | |
| | | TRSTn | |
| | | TDI | |
| | | TMS | |

PP3V3_S5
PLACE_NEAR=J1800.48:2.54MM
R1804 1K 5% 1/20W MF 201 — XDP:YES

PM_RSMRST_L — R1800 1K 5% 1/20W MF 201 — XDP:YES — PLACE_NEAR=U1200.H25:2.54MM
PM_PWRBTN_L — R1802 10 5% 1/20W MF 201 — XDP:YES — PLACE_NEAR=U1200.K22:5MM
SPI_MOSI_R — R1803 1.5K 5% 1/20W MF 201 — XDP:YES — PLACE_NEAR=U1200.D21:10MM

XDP_CPU_TCK
XDP_PCH_JTAGX — R1835 0 5% 1/20W MF 0201 — XDP:YES — PLACE_NEAR=J1800.58:28MM

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — XDP:YES — PLACE_NEAR=J1800.44:28MM
C1800 0.1UF 10% 6.3V CERM-X5R 0201 — XDP:YES — PLACE_NEAR=J1800.42:28MM
C1801 0.1UF 10% 6.3V CERM-X5R 0201 — XDP:YES — PLACE_NEAR=J1800.43:28MM
C1806 0.3UF 10% 6.3V CERM-X5R 0201 — XDP:YES — PLACE_NEAR=J1800.47:28MM

PP1V05_S0SW

| Signal | Resistor | Value | Notes |
|---|---|---|---|
| XDP_PCH_TDO | R1890 | 100 | PLACE_NEAR=U1200.AM16:28MM |
| XDP_PCH_TDI | R1891 | 51 | PLACE_NEAR=U1200.AR18:28MM |
| XDP_PCH_TMS | R1892 | 51 | PLACE_NEAR=U1200.AL14:28MM |
| XDP_CPU_TDO | R1810 | 100 | PLACE_NEAR=U0500.BT28:28MM |
| XDP_CPU_TCK | R1813 | 51 | PLACE_NEAR=U0500.BR28:28MM |
| XDP_PCH_TCK | R1897 | 51 | PLACE_NEAR=U1200.AP17:28MM |
| XDP_PCH_TRST_L | R1898 | 51 | PROPER WAY TO TERMINATE? |

All: XDP:YES, 5% 1/20W MF 201

NOSTUFF

R1830 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.E8:2.54MM

R1806 0 5% 1/20W MF 0201 — XDP:YES — PM_SYSRST_L

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

| Resistor | Value | Signal | Place near |
|---|---|---|---|
| R1821 | 0 | XDP_CPU_TDO | PLACE_NEAR=J1800.51:2.54MM |
| R1822 | 0 | XDP_CPU_TRST_L | PLACE_NEAR=J1800.53:2.54MM |
| R1823 | 0 | XDP_CPU_TDI | PLACE_NEAR=J1800.55:2.54MM |
| R1824 | 0 | XDP_CPU_TMS | PLACE_NEAR=J1800.57:2.54MM |

All: 5% 1/20W MF 0201, XDP:YES

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PP1V8_S5
C1830 0.1UF 10% 10V X5R-CERM 0201 — XDP:YES
U1830 74AUP1G07GF SOT891 — XDP:YES
SPI_IO2_STRAP_L — R1831 1.5K 5% 1/20W MF 201 — XDP:YES — NO_XNET_CONNECTION — SPI_IO<2> (STRAP TO PCH)
PLACE_NEAR=U1830.4:7.54MM
PLACE_NEAR=U1830.4:2.54MM — R1832 49.9 1% 1/20W MF 201 — NOSTUFF — NO_XNET_CONNECTION
XDP_PRESENT_L

PP1V8_S5 — R1850 100K 5% 1/20W MF 201 — XDP:YES

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

## PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

### PCH/XDP Signals

| Signal | Place side | Test point |
|---|---|---|
| XDP_PCH_OBSDATA_A0 | PLACE_SIDE=BOTTOM | TP1810 |
| XDP_PCH_OBSDATA_A1 | PLACE_SIDE=BOTTOM | TP1811 |
| XDP_PCH_OBSDATA_A2 | PLACE_SIDE=BOTTOM | TP1812 |
| XDP_PCH_OBSDATA_A3 | PLACE_SIDE=BOTTOM | TP1813 |
| XDP_PCH_OBSDATA_B0 | PLACE_SIDE=BOTTOM | TP1814 |
| XDP_PCH_OBSDATA_B1 | PLACE_SIDE=BOTTOM | TP1815 |
| XDP_PCH_OBSDATA_B2 | PLACE_SIDE=BOTTOM | TP1816 |
| XDP_PCH_OBSDATA_B3 | PLACE_SIDE=BOTTOM | TP1817 |
| XDP_PCH_OBSFN_C0 | PLACE_SIDE=BOTTOM | TP1818 |
| XDP_USB_EXTA_OC_L | PLACE_SIDE=BOTTOM | TP1820 |
| XDP_USB_EXTB_OC_L | PLACE_SIDE=BOTTOM | TP1821 |
| XDP_USB_EXTC_OC_L | PLACE_SIDE=BOTTOM | TP1822 |
| XDP_USB_EXTD_OC_L | PLACE_SIDE=BOTTOM | TP1823 |
| XDP_PCH_OBSDATA_D0 | PLACE_SIDE=BOTTOM | TP1824 |
| XDP_PCH_OBSDATA_D1 | PLACE_SIDE=BOTTOM | TP1825 |

### Non-XDP Signals

| Signal | Place side | Test point |
|---|---|---|
| XDP_JTAG_ISP_TDO | PLACE_SIDE=BOTTOM | TP1819 |
| XDP_JTAG_ISP_TCK | PLACE_SIDE=BOTTOM | TP1826 |
| XDP_JTAG_ISP_TDI | PLACE_SIDE=BOTTOM | TP1827 |

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: 051-02888 — SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 18 OF 200
SHEET: 18 OF 131

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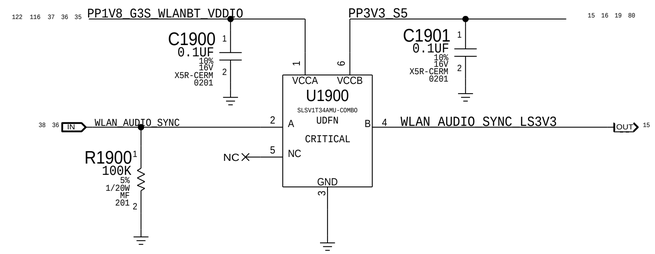
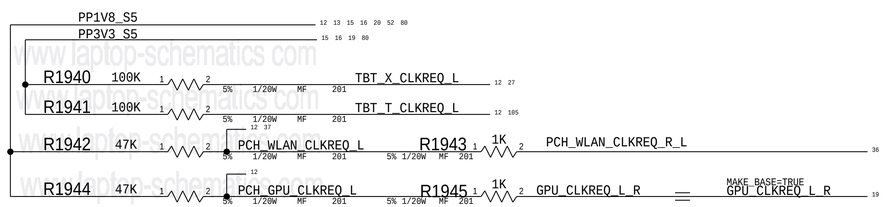
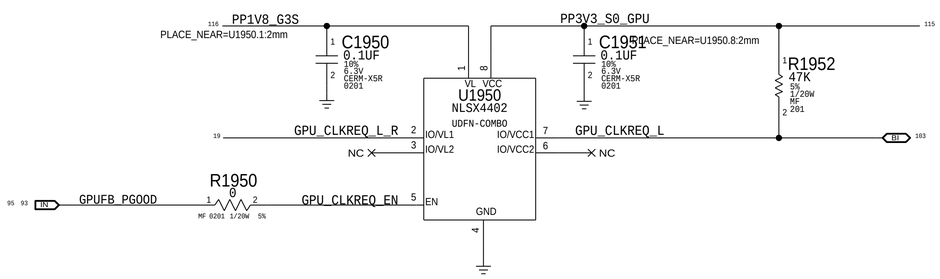



Will be reomved

PCIE CLKREQS

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BOM_COST_GROUP=CPU & CHIPSET

FAB#:RC315

PAGE TITLE
Chipset Support 1

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 19 OF 200

SHEET 19 OF 131

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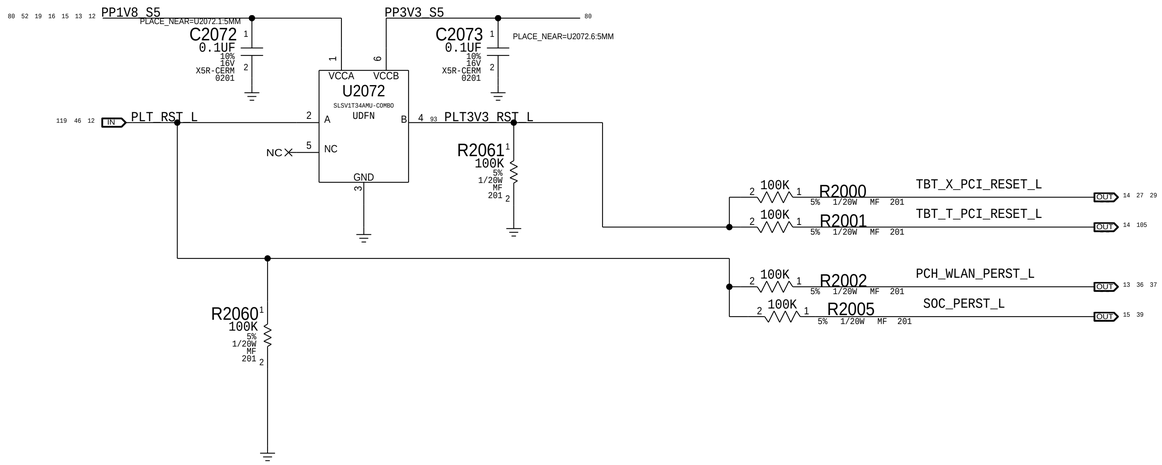
## Platform Reset Connections




## NC ALIASES 3

NC_PCH_CLK32K_RTCX2 — MAKE_BASE=TRUE — NC_PCH_CLK32K_RTCX2

## SIGNAL ALIASES

PCH_DISPA_BCLK — MAKE_BASE=TRUE — PCH_DISPA_BCLK

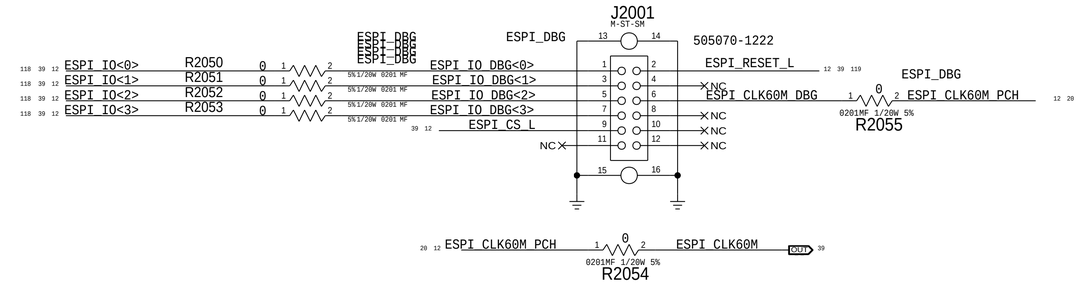
PCH_DISPA_SDI — MAKE_BASE=TRUE — PCH_DISPA_SDI

PCH_DISPA_SDO — MAKE_BASE=TRUE — PCH_DISPA_SDO

NC_ITPXDP_CLK100MN — TRUE — NC_ITPXDP_CLK100MN

NC_ITPXDP_CLK100MP — TRUE — NC_ITPXDP_CLK100MP

## eSPI Analyzer
## Placement study first







BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 2

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DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 20 OF 200
SHEET 20 OF 131

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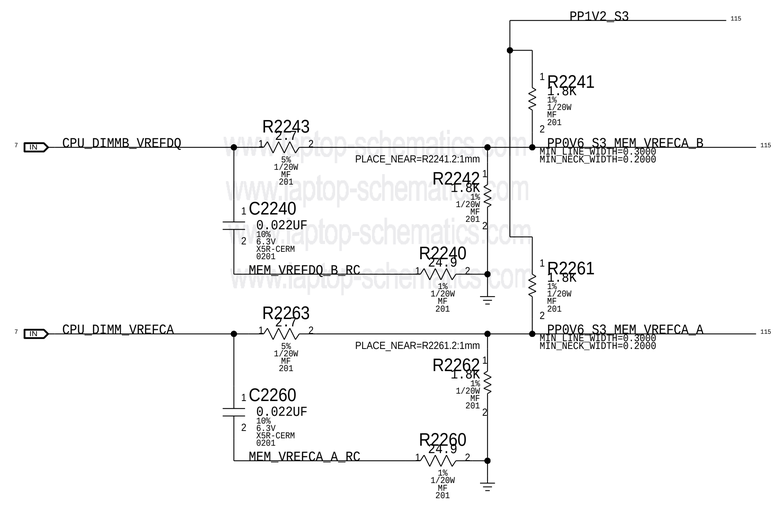
# CPU-Based Margining
## VRef Dividers

```
DDR4 VDDQ = 1.2V
----------------
MIMINUM Step Size = 0.50% * VDDQ = 6.0mV per step
TYPICAL Step Size = 0.65% * VDDQ = 7.8mV per step
MAXIMUM Step Size = 0.80% * VDDQ = 9.6mV per step

 KBL PLATFORM GUIDE Page.102 FOR DDR4 X8 MEMORY DOWN
 ---------------------------------------------------
 DDR0_VREF_DQ = Not Used
 DDR1_VREF_DQ = Reference For Channel B
 DDR_vREF_CA = Reference For Channel A
```




BOM_COST_GROUP=DRAM

| | |
|---|---|
| PAGE TITLE | DDR4 VREF Margining |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
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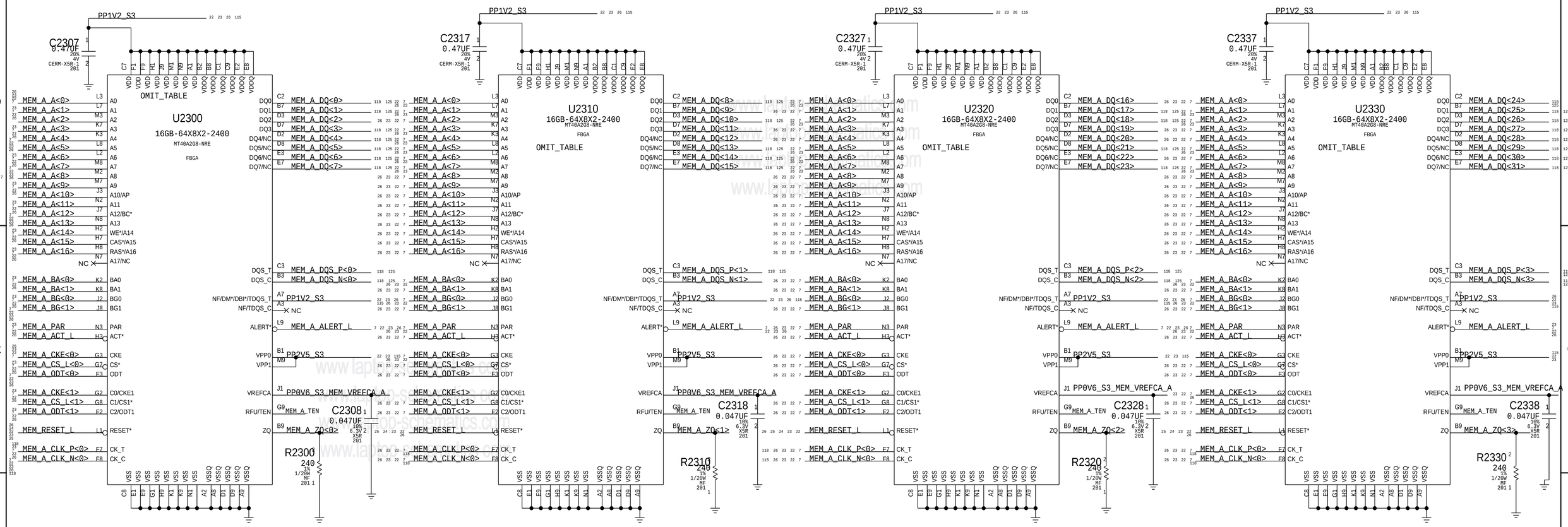
| | SHEET 21 OF 131 |

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PAGE TITLE

# DDR4 SDRAM Channel A 1

Apple Inc.

| | |
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| DRAWING NUMBER | 051-02888 |
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| BRANCH | EVT |
| PAGE | 23 OF 200 |
| SHEET | 22 OF 131 |

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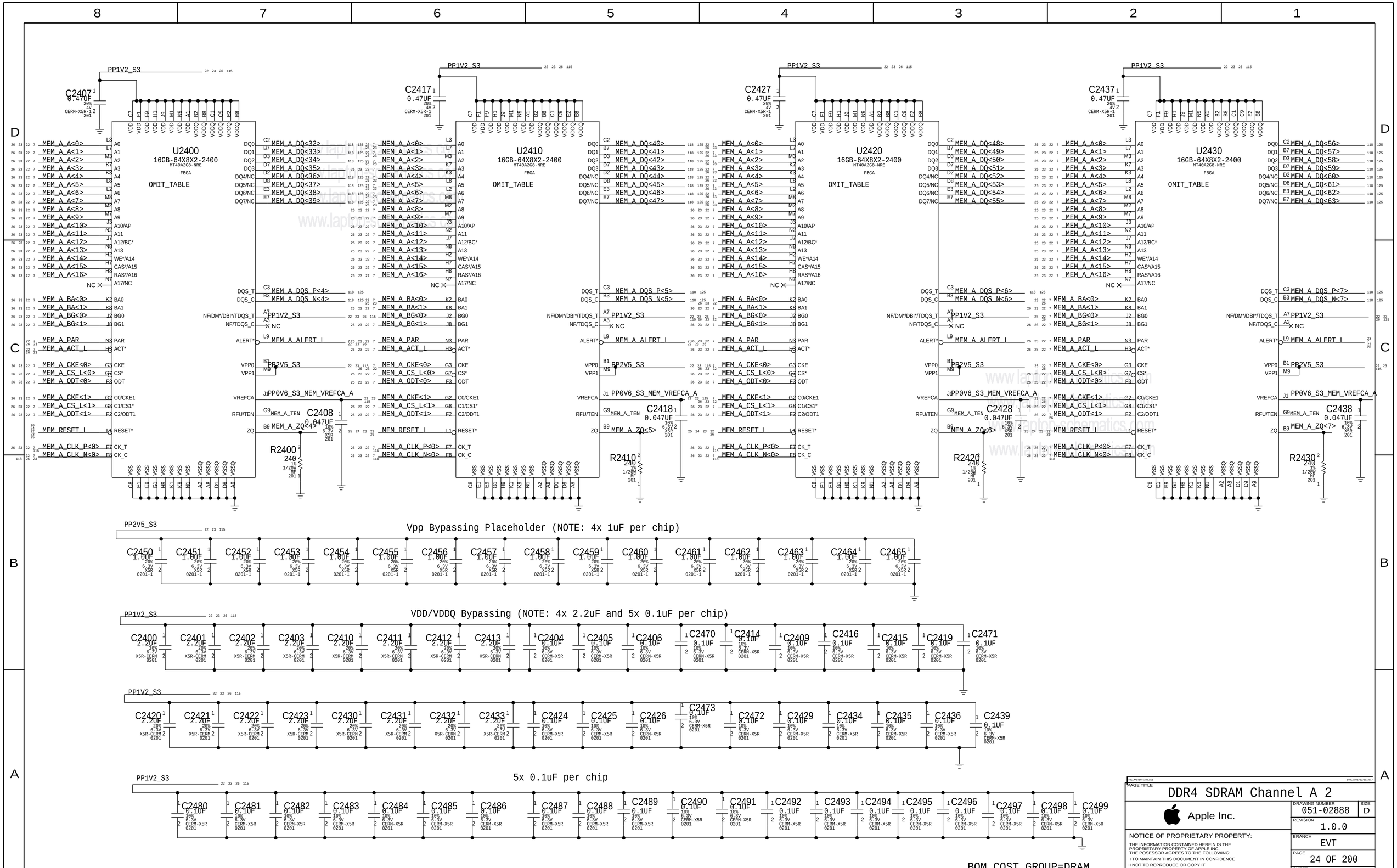


PAGE TITLE

# DDR4 SDRAM Channel A 2

Apple Inc.

| | |
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| SHEET | 23 OF 131 |

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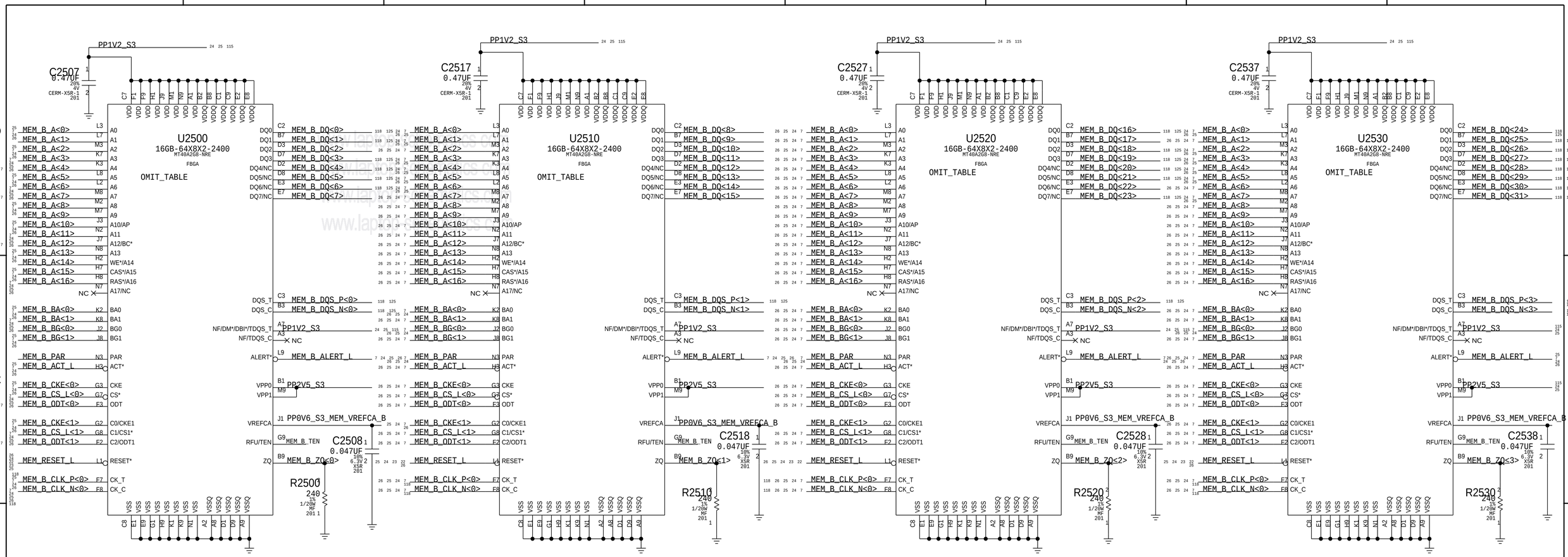


PAGE TITLE

# DDR4 SDRAM Channel B 1

Apple Inc.

| | |
|---|---|
| DRAWING NUMBER | 051-02888 |
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| SHEET | 24 OF 131 |

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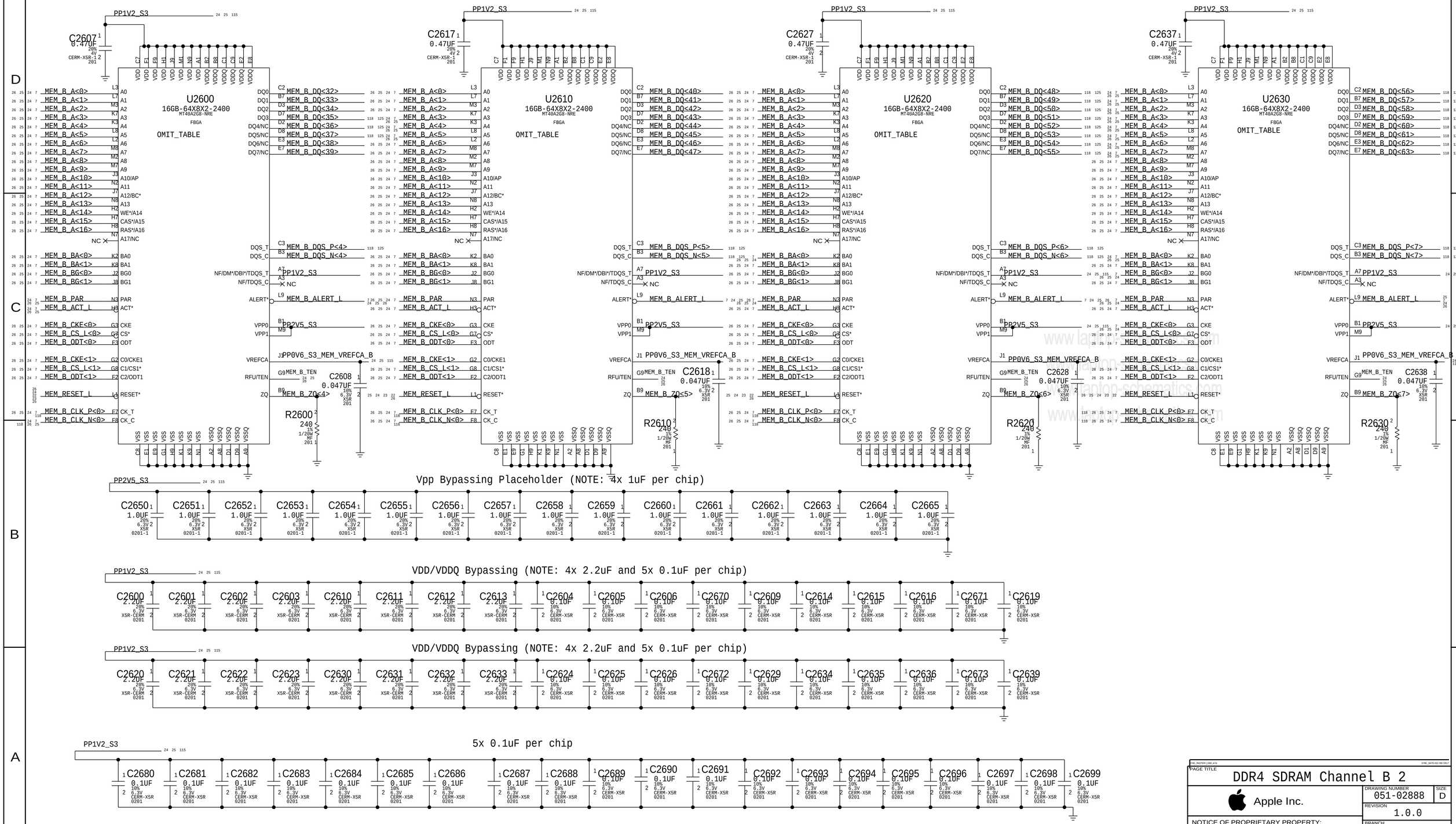


| | |
|---|---|
| PAGE TITLE | DDR4 SDRAM Channel B 2 |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

PP0V6_S0_DDRVTT

C2701,C2721 FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

| | | | |
|---|---|---|---|
| MEM_A_A<0> | R2700 | 36 | |
| MEM_A_A<1> | R2701 | 36 | |
| MEM_A_A<2> | R2702 | 36 | |
| MEM_A_A<3> | R2703 | 36 | |
| MEM_A_A<4> | R2704 | 36 | |
| MEM_A_A<5> | R2705 | 36 | |
| MEM_A_A<6> | R2706 | 36 | |
| MEM_A_A<7> | R2707 | 36 | |
| MEM_A_A<8> | R2708 | 36 | |
| MEM_A_A<9> | R2709 | 36 | |
| MEM_A_A<10> | R2710 | 36 | |
| MEM_A_A<11> | R2711 | 36 | |
| MEM_A_A<12> | R2712 | 36 | |
| MEM_A_A<13> | R2713 | 36 | |
| MEM_A_A<14> | R2714 | 36 | |
| MEM_A_A<15> | R2715 | 36 | |
| MEM_A_A<16> | R2716 | 36 | |
| MEM_A_BA<0> | R2717 | 36 | |
| MEM_A_BA<1> | R2718 | 36 | |
| MEM_A_BG<0> | R2719 | 36 | |
| MEM_A_BG<1> | R2720 | 36 | |
| MEM_A_CS_L<0> | R2721 | 36 | |
| MEM_A_CS_L<1> | R2722 | 36 | |
| MEM_A_CKE<0> | R2723 | 36 | |
| MEM_A_CKE<1> | R2724 | 36 | |
| MEM_A_ODT<0> | R2725 | 36 | |
| MEM_A_ODT<1> | R2726 | 36 | |
| MEM_A_ACT_L | R2727 | 36 | |
| MEM_A_PAR | R2728 | 36 | |

C2700 2.2UF 20% 4V X5R-CERM 0201
C2701 12PF 5% NPO-C0G 0201 25V
C2702 2.2UF 20% 4V X5R-CERM 0201
C2703 2.2UF 20% 4V X5R-CERM 0201
C2704 2.2UF 20% 4V X5R-CERM 0201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2710 0.47UF 20% 4V CERM-X5R-1 201

PP0V6_S0_DDRVTT

| | | | |
|---|---|---|---|
| MEM_B_A<0> | R2770 | 36 | |
| MEM_B_A<1> | R2771 | 36 | |
| MEM_B_A<2> | R2772 | 36 | |
| MEM_B_A<3> | R2773 | 36 | |
| MEM_B_A<4> | R2774 | 36 | |
| MEM_B_A<5> | R2775 | 36 | |
| MEM_B_A<6> | R2776 | 36 | |
| MEM_B_A<7> | R2777 | 36 | |
| MEM_B_A<8> | R2778 | 36 | |
| MEM_B_A<9> | R2779 | 36 | |
| MEM_B_A<10> | R2780 | 36 | |
| MEM_B_A<11> | R2781 | 36 | |
| MEM_B_A<12> | R2782 | 36 | |
| MEM_B_A<13> | R2783 | 36 | |
| MEM_B_A<14> | R2784 | 36 | |
| MEM_B_A<15> | R2785 | 36 | |
| MEM_B_A<16> | R2786 | 36 | |
| MEM_B_BA<0> | R2787 | 36 | |
| MEM_B_BA<1> | R2788 | 36 | |
| MEM_B_BG<0> | R2789 | 36 | |
| MEM_B_BG<1> | R2790 | 36 | |
| MEM_B_CS_L<0> | R2791 | 36 | |
| MEM_B_CS_L<1> | R2792 | 36 | |
| MEM_B_CKE<0> | R2793 | 36 | |
| MEM_B_CKE<1> | R2794 | 36 | |
| MEM_B_ODT<0> | R2795 | 36 | |
| MEM_B_ODT<1> | R2796 | 36 | |
| MEM_B_ACT_L | R2797 | 36 | |
| MEM_B_PAR | R2798 | 36 | |

C2720 2.2UF 20% 4V X5R-CERM 0201
C2721 12PF 5% NPO-C0G 0201 25V
C2722 2.2UF 20% 4V X5R-CERM 0201
C2723 2.2UF 20% 4V X5R-CERM 0201
C2724 2.2UF 20% 4V X5R-CERM 0201
C2725 0.47UF 20% 4V CERM-X5R-1 201
C2726 0.47UF 20% 4V CERM-X5R-1 201
C2727 0.47UF 20% 4V CERM-X5R-1 201
C2728 0.47UF 20% 4V CERM-X5R-1 201
C2730 0.47UF 20% 4V CERM-X5R-1 201

MEM_A_TEN — R2752 0 5% 1/20W MF 0201 — MEM_A_TEN_R — TP2700 TP-P5
R2753 100 5% 1/20W MF 201
NOSTUFF C2752 0.47UF 20% 4V CERM-X5R-1 201

MEM_B_TEN — R2754 0 5% 1/20W MF 0201 — MEM_B_TEN_R — TP2701 TP-P5
R2755 100 5% 1/20W MF 201
NOSTUFF C2753 0.47UF 20% 4V CERM-X5R-1 201

## MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0> — R2750 30 5% 1/20W MF 201 — MEM_A_CLK0_TERM_R — C2751 0.01UF 10% 25V X5R-CERM 0201 — PP0V6_S0_DDRVTT
PLACE_NEAR=U2430.F8:8mm
NOSTUFF C2750 3300PF 10% 10V X7R-CERM 0201
PLACE_NEAR=U2430.F8:10mm
MEM_A_CLK_P<0> — R2751 30 5% 1/20W MF 201
PLACE_NEAR=U2430.F7:8mm

MEM_B_CLK_N<0> — R2760 30 5% 1/20W MF 201 — MEM_B_CLK0_TERM_R — C2761 0.01UF 10% 25V X5R-CERM 0201 — PP0V6_S0_DDRVTT
PLACE_NEAR=U2630.F8:8mm
NOSTUFF C2760 3300PF 10% 10V X7R-CERM 0201
PLACE_NEAR=U2630.F8:10mm
MEM_B_CLK_P<0> — R2761 30 5% 1/20W MF 201
PLACE_NEAR=U2630.F7:8mm

| | | |
|---|---|---|
| NC_MEM_A_CLK_N<1> | MAKE_BASE=TRUE | NC_MEM_A_CLK_N<1> |
| NC_MEM_A_CLK_P<1> | MAKE_BASE=TRUE | NC_MEM_A_CLK_P<1> |
| NC_MEM_A_CKE<2> | MAKE_BASE=TRUE | NC_MEM_A_CKE<2> |
| NC_MEM_A_CKE<3> | MAKE_BASE=TRUE | NC_MEM_A_CKE<3> |
| NC_MEM_B_CLK_N<1> | MAKE_BASE=TRUE | NC_MEM_B_CLK_N<1> |
| NC_MEM_B_CLK_P<1> | MAKE_BASE=TRUE | NC_MEM_B_CLK_P<1> |
| NC_MEM_B_CKE<2> | MAKE_BASE=TRUE | NC_MEM_B_CKE<2> |
| NC_MEM_B_CKE<3> | MAKE_BASE=TRUE | NC_MEM_B_CKE<3> |

PP1V2_S3

MEM_A_ALERT_L — R2730 51 1% 1/20W MF 201
MEM_B_ALERT_L — R2731 51 1% 1/20W MF 201
R2733 470 1% 1/20W MF 201 — MEM_RESET_L
PCH_DRAM_RESET_L — R2732 0 5% 1/20W MF 0201
NOSTUFF C2732 0.1UF 10% 6.3V CERM-X5R 0201

BOM_COST_GROUP=DRAM

PAGE TITLE: DDR4 Termination

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DRAWING NUMBER: 051-02888 SIZE: D
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BRANCH: EVT
PAGE: 27 OF 200
SHEET: 26 OF 131

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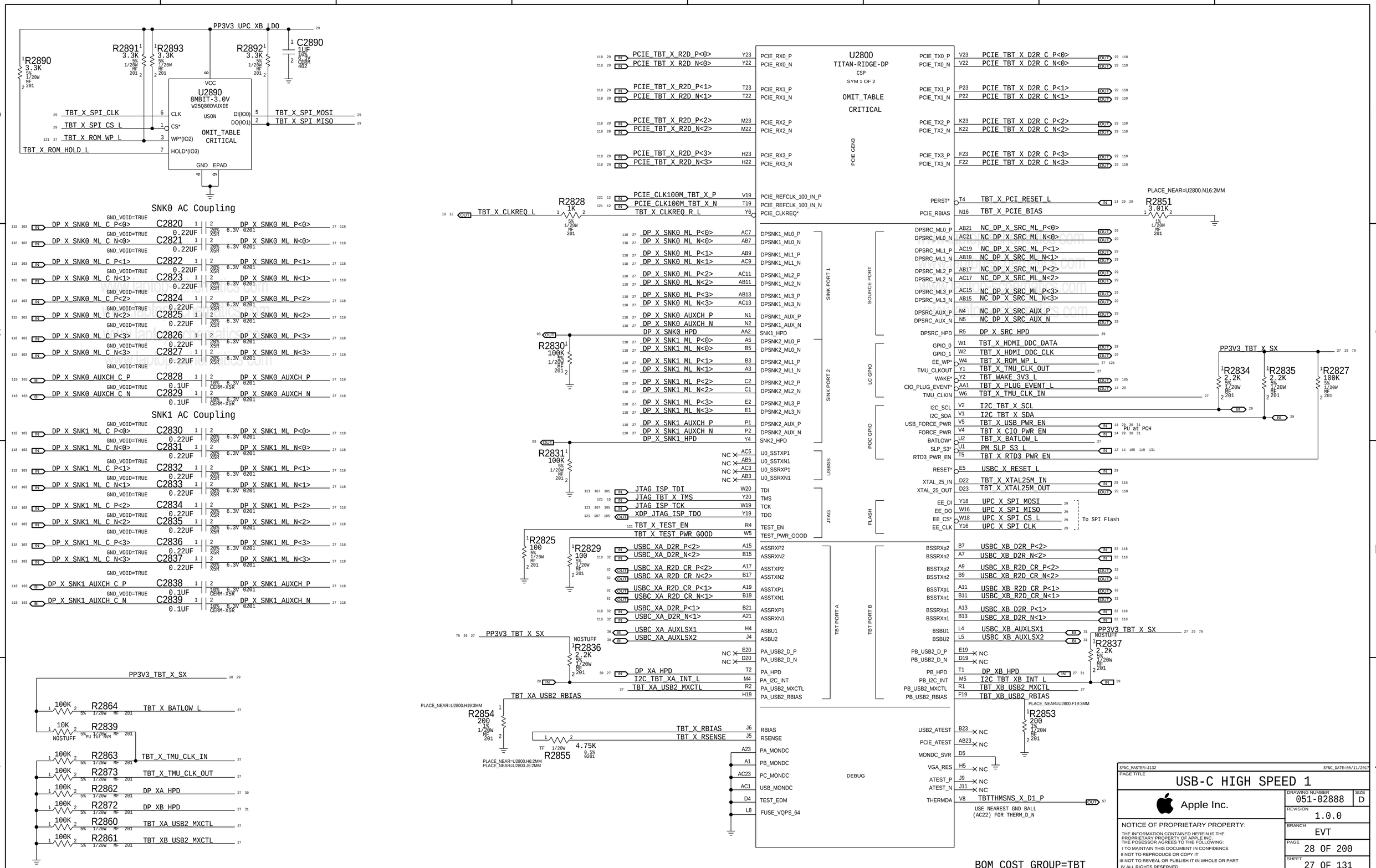
PP3V3_UPC_XB_LDO
R2890 3.3K
R2891 3.3K
R2893 3.3K
R2892 3.3K
C2890 1UF
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
U2800 TITAN-RIDGE-DP CSP SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
SINK PORT 1
SINK PORT 2
SOURCE PORT
LC GPIO
POC GPIO
USB5S
JTAG
FLASH
TBT PORT A
TBT PORT B
DEBUG
TBT_X_CLKREQ_L
R2828 1K
PLACE_NEAR=U2800.N16:2MM
R2851 3.01K
R2830 100K
R2831 100K
R2825 100
R2829 100
R2836 2.2K
R2854 200
R2855 4.75K
R2834 2.2K
R2835 2.2K
R2827 100K
R2837 2.2K
R2853 200
PU at PCH
To SPI Flash
PP3V3_TBT_X_SX
R2864 100K
R2839 10K
R2863 100K
R2873 100K
R2862 100K
R2872 100K
R2860 100K
R2861 100K
TBT_X_BATLOW_L
TBT_X_TMU_CLK_IN
TBT_X_TMU_CLK_OUT
DP_XA_HPD
DP_XB_HPD
TBT_XA_USB2_MXCTL
TBT_XB_USB2_MXCTL
BOM_COST_GROUP=TBT
SYNC_MASTER=J132
SYNC_DATE=05/11/2017
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 28 OF 200
SHEET 27 OF 131
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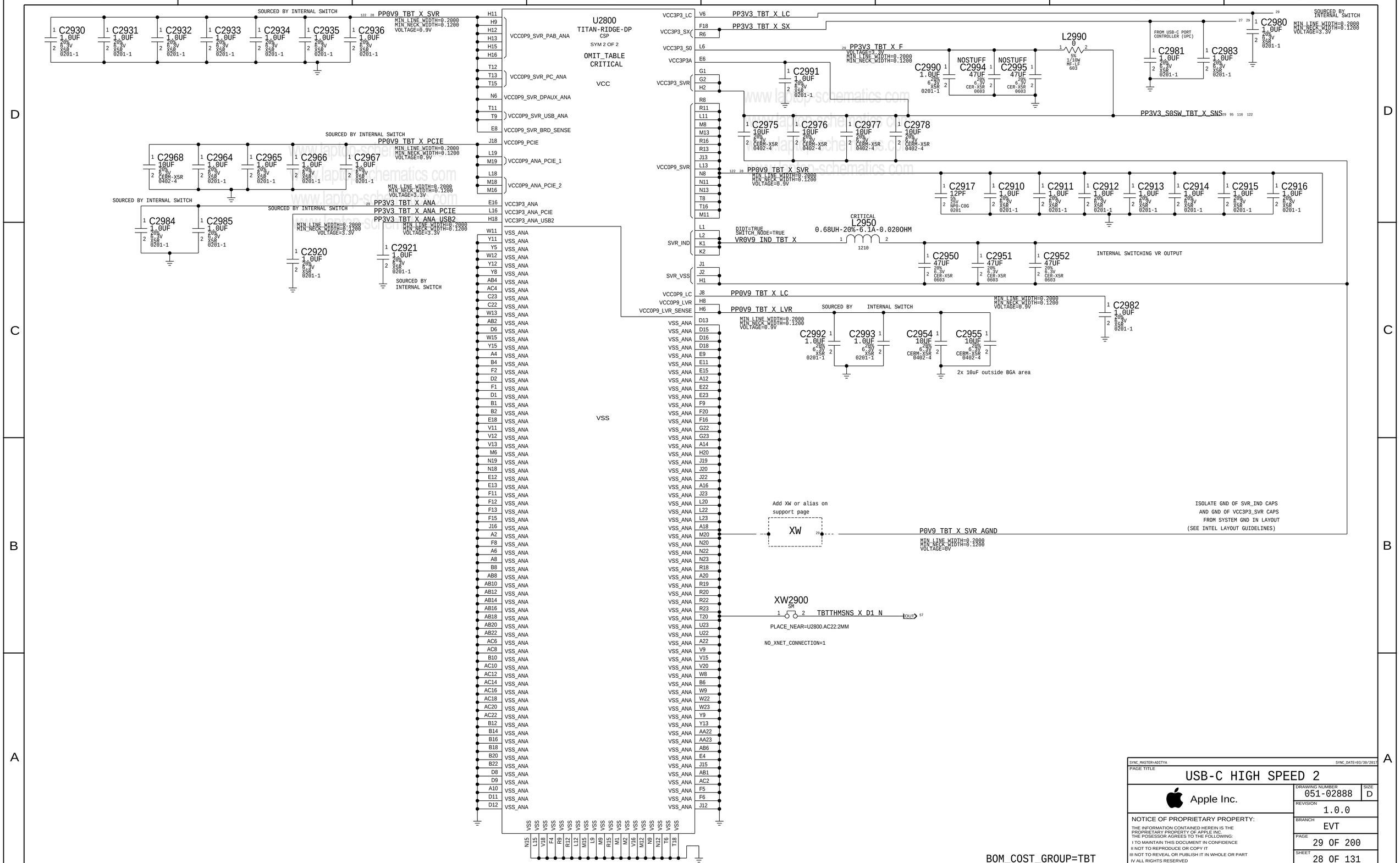


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PAGE TITLE
USB-C HIGH SPEED 2

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PAGE 29 OF 200
SHEET 28 OF 131

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## TBT WAKE LEVEL SHIFTER

PP3V3_G3H_RTC_X
PP1V8_SLPS2R
Q3001 DMN32D2LFB4 PDFN1006H4-3
R3065 100K 5% 1/20W MF 201
SMC HAS IPU
TBT_WAKE_L → TBT_WAKE_3V3_L

## DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD — R3040 100K 1/20W 5% MF 201

| | | |
|---|---|---|
| =DP_X_SRC_ML_P<3..0> | NC_DP_X_SRC_ML_P<3..0> | MAKE_BASE=TRUE NO_TEST=1 |
| =DP_X_SRC_ML_N<3..0> | NC_DP_X_SRC_ML_N<3..0> | MAKE_BASE=TRUE NO_TEST=1 |
| NC_DP_X_SRC_AUX_P | NC_DP_X_SRC_AUX_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_DP_X_SRC_AUX_N | NC_DP_X_SRC_AUX_N | MAKE_BASE=TRUE NO_TEST=1 |

## FUSES FOR UPC

PLACE_NEAR=Q3100:5MM
CRITICAL
0603 F3000 6AMP-32V-0.00950OHM
PP20V_USBC_XA_VBUS — PP20V_USBC_XA_VBUS_F

PLACE_NEAR=Q3200:5MM
CRITICAL
0603 740S0135 F3001 6AMP-32V-0.00950OHM
PP20V_USBC_XB_VBUS — PP20V_USBC_XB_VBUS_F

## 25MHz xtal

TBT_X_XTAL25M_OUT
to/from Ridge
CRITICAL Y3000 25MHZ-25PPM-20PF-500HM 2.00X1.60-SM
C3002 20PF 5% 25V C0G 0201
C3003 20PF 5% 25V C0G 0201
TBT_X_XTAL25M_IN

## TR/ACE SPI BUS SERIES R's

| | | | |
|---|---|---|---|
| TBT_X_SPI_CLK | R3094 100 | TBT_X_SPI_CLK_DBG | |
| TBT_X_SPI_CS_L | R3095 15 | UPC_XB_SPI_CLK | Ace |
| TBT_X_SPI_MOSI | R3096 15 | UPC_XB_SPI_CS_L | Ace |
| TBT_X_SPI_MISO | R3097 15 | UPC_XB_SPI_MOSI | Ace |
| ROM | R3098 15 | UPC_XB_SPI_MISO | Ace |
| | R3090 15 | UPC_X_SPI_CLK | AR |
| | R3091 15 | UPC_X_SPI_CS_L | AR |
| | R3092 15 | UPC_X_SPI_MOSI | AR |
| | R3093 15 | UPC_X_SPI_MISO | AR |

## Ridge and ACE PDs

| | | |
|---|---|---|
| UPC_X_5V_EN | R3032 | 100K |
| TBT_XA_LSTX | R3020 | 1M |
| TBT_XA_LSRX | R3021 | 1M |
| TBT_XB_LSTX | R3022 | 1M |
| TBT_XB_LSRX | R3023 | 1M |
| USB_UPC_XA_P | R3024 | 1M |
| USB_UPC_XA_N | R3025 | 1M |

## RIDGE ARKANOID CONN

Place on bottom
USBC_DBG — J3001 M-ST-SM 505070-1222

| | | |
|---|---|---|
| TBT_X_PLUG_EVENT_L | 1–2 | TBT_X_PCI_RESET_L |
| TBT_WAKE_3V3_L | 3–4 | USBC_X_RESET_L |
| TBT_X_CIO_PWR_EN | 5–6 | PP3V3_TBT_X_SX |
| TBT_X_USB_PWR_EN | 7–8 | PP3V3_TBT_T_ANA_PCIE |
| TBT_POC_RESET | 9–10 | PP3V3_TBT_X_ANA |
| PP3V3_TBT_X_F | 11–12 | PP3V3_TBT_X_LC |
| | 15–16 | |

## ACE ARKANOID CONN

Place on bottom
USBC_DBG — J3000 M-ST-SM 505070-1222

| | | |
|---|---|---|
| CKPLUS_WAIVE=I2C_PULLUP | 1–2 | I2C_TBT_XA_INT_L |
| CKPLUS_WAIVE=I2C_PULLUP | 3–4 | I2C_TBT_X_SDA |
| I2C_UPC_X_SDA2 | 5–6 | I2C_TBT_X_SCL |
| UPC_I2C_INT_L | 7–8 | I2C_UPC_XA_DBG_CTL_SDA |
| TBT_X_SPI_CLK_DBG | 9–10 | I2C_UPC_XA_DBG_CTL_SCL |
| UPC_XA_UART_TX | 11–12 | UPC_XA_UART_RX |
| | 15–16 | |

## USBC DEBUG CONN

| | | |
|---|---|---|
| TBT_X_SPI_CLK_DBG | IN | 29 |
| UPC_XB_SPI_CLK | IN | 31 |
| UPC_XB_SPI_CS_L | IN | 31 |
| UPC_XB_SPI_MOSI | IN | 31 |
| UPC_XB_SPI_MISO | OUT | 31 |
| UPC_X_SPI_CLK | IN | 27 29 |
| UPC_X_SPI_CS_L | IN | 27 29 |
| UPC_X_SPI_MOSI | IN | 27 29 |
| UPC_X_SPI_MISO | OUT | 27 29 |

## NC ALIASES / NO TEST

NO_TEST=1
NC_UPC_XB_I2C_ADDR
NC_USBC_XA_USB_BOTP — MAKE_BASE=TRUE NC_USBC_XA_USB_BOTP
NC_USBC_XA_USB_BOTN — MAKE_BASE=TRUE NC_USBC_XA_USB_BOTN NO_TEST=1

## DCI / PCH USB3

USB3_EXTA_R2D_C_P — C3020 0.1UF 10% 16V X5R-CERM 0201
USB3_EXTA_R2D_C_N — C3021 0.1UF 10% 16V X5R-CERM 0201

PP3V3_G3H_RTC_X — C3022 0.1UF 10% 16V X5R-CERM 0201

## U3000 PI3USB32324

VDD 20; GND; EPAD

| | | | |
|---|---|---|---|
| USB3_EXTA_D2R_P | PCH_USB3_RX_P | USB2_RP_P | USB_DBG_PCH_XA_F_P |
| USB3_EXTA_D2R_N | PCH_USB3_RX_N | USB2_RP_N | USB_DBG_PCH_XA_F_N |
| USB3_EXTA_R2D_P | PCH_USB3_TX_P | USB2_B_P | USBC_XA_USB_DBG_BOT_P |
| USB3_EXTA_R2D_N | PCH_USB3_TX_N | USB2_B_N | USBC_XA_USB_DBG_BOT_N |
| USB_SOC_TYPEC_P | USB2_EP_P | USB2_T_N | USBC_XA_USB_DBG_TOP_N |
| USB_SOC_TYPEC_N | USB2_EP_N | USB2_T_P | USBC_XA_USB_DBG_TOP_P |
| SWD_SOC_SWCLK | SWCLK | SDA | I2C_UPC_XA_DBG_CTL_SDA |
| SWD_SOC_SWDIO | SWDIO | SCL | I2C_UPC_XA_DBG_CTL_SCL |
| USBC_XA_USB_TOP_P | ANALOG1 | DEBUG1 | UPC_XA_DBG1 |
| USBC_XA_USB_TOP_N | ANALOG2 | DEBUG2 | UPC_XA_DBG2 |

USB2_UPC_XA_P — L3000 90-OHM-0.1A EXCX4CE
USB2_UPC_XA_N — PLACE_NEAR=U3000:5mm

## ACE A RPD STRAPPING

USBC_XA_CC1 — USBC_XA_CC1 MAKE_BASE=TRUE
USBC_XA_CC2 — USBC_XA_CC2 MAKE_BASE=TRUE

## GND ALIASES

MAKE_BASE=TRUE
GND

## RIDGE 0.9V SVR XW

P0V9_TBT_X_SVR_AGND — XW3000 SM
NO_XNET_CONNECTION=1

## ACE B RPD STRAPPING

USBC_XB_CC1 — USBC_XB_CC1 MAKE_BASE=TRUE
USBC_XB_CC2 — USBC_XB_CC2 MAKE_BASE=TRUE

## SIGNAL ALIASES

| | | |
|---|---|---|
| UPC_X_5V_EN | UPC_X_5V_EN | MAKE_BASE=TRUE |
| USB2_UPC_XB_P | USB2_UPC_XB_P | MAKE_BASE=TRUE |
| USB2_UPC_XB_N | USB2_UPC_XB_N | MAKE_BASE=TRUE |
| USB2_UPC_XA_P | USB2_UPC_XA_P | MAKE_BASE=TRUE |
| USB2_UPC_XA_N | USB2_UPC_XA_N | MAKE_BASE=TRUE |
| UPC_PMU_RESET | UPC_PMU_RESET | MAKE_BASE=TRUE |
| USBC_X_RESET_L | USBC_X_RESET_L | MAKE_BASE=TRUE |
| UPC_X_SPI_CLK | UPC_X_SPI_CLK | MAKE_BASE=TRUE |
| UPC_X_SPI_CS_L | UPC_X_SPI_CS_L | MAKE_BASE=TRUE |
| UPC_X_SPI_MOSI | UPC_X_SPI_MOSI | MAKE_BASE=TRUE |
| UPC_X_SPI_MISO | UPC_X_SPI_MISO | MAKE_BASE=TRUE |
| UPC_T_SPI_CLK | UPC_T_SPI_CLK | MAKE_BASE=TRUE |
| UPC_T_SPI_CS_L | UPC_T_SPI_CS_L | MAKE_BASE=TRUE |
| UPC_T_SPI_MOSI | UPC_T_SPI_MOSI | MAKE_BASE=TRUE |
| UPC_T_SPI_MISO | UPC_T_SPI_MISO | MAKE_BASE=TRUE |

TBT_POC_RESET — TBT_POC_RESET MAKE_BASE=TRUE
UPC_XA_FAULT_L — R3078 0 5% MF 1/20W 0201 — XDP_USB_EXTA_OC_L
UPC_XB_FAULT_L — R3079 0 5% MF 1/20W 0201 — XDP_USB_EXTB_OC_L
TP_USBC_XA_RESET_L — TP_USBC_XA_RESET_L MAKE_BASE=TRUE
TBT_X_HDMI_DDC_DATA — TBT_X_HDMI_DDC_DATA MAKE_BASE=TRUE
TBT_X_HDMI_DDC_CLK — TBT_X_HDMI_DDC_CLK MAKE_BASE=TRUE

## POWER ALIASES

| | | |
|---|---|---|
| PP3V3_UPC_XB_LDO | PP3V3_UPC_XB_LDO | MAKE_BASE=TRUE |
| PP3V3_UPC_XA_LDO | PP3V3_UPC_XA_LDO | MAKE_BASE=TRUE |
| PP20V_USBC_XA_VBUS | PP20V_USBC_XA_VBUS | MAKE_BASE=TRUE |
| PP20V_USBC_XB_VBUS | PP20V_USBC_XB_VBUS | MAKE_BASE=TRUE |
| PPDCIN_G3H | PPDCIN_G3H | MAKE_BASE=TRUE |
| PP5V_S4_X_USBC | PP5V_S4_X_USBC | MAKE_BASE=TRUE |
| PP5V_S4_X_USBC | | |
| PP5V_S4_X_USBC | | |
| PP3V3_S0SW_TBT_X_SNS | PP3V3_S0SW_TBT_X_SNS | MAKE_BASE=TRUE |
| PP3V3_TBT_X_SX | PP3V3_TBT_X_SX | MAKE_BASE=TRUE |
| PP3V3_TBT_X_SX | | |
| PP3V3_TBT_X_SX | | |
| PP1V8_SLPS2R | PP1V8_SLPS2R | |
| PP1V8_SLPS2R | | |

## DEBUG ALIASES

| | | |
|---|---|---|
| PCH_UART_DEBUG_R2D | PCH_UART_DEBUG_R2D | MAKE_BASE=TRUE |
| PCH_UART_DEBUG_D2R | PCH_UART_DEBUG_D2R | MAKE_BASE=TRUE |
| SOC_DFU_STATUS | SOC_DFU_STATUS | MAKE_BASE=TRUE |
| SOC_FORCE_DFU | SOC_FORCE_DFU | MAKE_BASE=TRUE |

SWD_SOC_SWCLK — R3076 0 5% MF 1/20W 0201 — UPC_XB_DBG3
PLACE_NEAR=U3000.24:5mm
SWD_SOC_SWDIO — R3077 0 5% MF 1/20W 0201 — UPC_XB_DBG4
PLACE_NEAR=U3000.23:5mm

## Diodes for USB2

USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P

PLACE_NEAR=U3000.19:10mm
PLACE_NEAR=U3000.18:10mm
PLACE_NEAR=U3000.15:10mm
PLACE_NEAR=U3000.16:10mm

BAS70LP DFN1006-2 D3001; BAS70LP DFN1006-2 D3002; BAS70LP DFN1006-2 D3003; BAS70LP DFN1006-2 D3004

## I2C SERIES R's

I2C_UPC_X_SDA2 — R3041 33 5% 1/20W MF 201 — I2C_UPC_SDA (PLACE_NEAR=U3900.J4:5mm)
I2C_UPC_X_SCL2 — R3042 33 5% 1/20W MF 201 — I2C_UPC_SCL (PLACE_NEAR=U3900.M3:10mm)

PP20V_USBC_XA_VBUS_F — R3080 30K 5% 1/20W MF 201 — SOC_USB_VBUS
D3080 BZT52C3V0LP DFN1006

## TBT to ACE

| TBT Alpine Ridge U2800 (MASTER) | | Pri ACE U3100 (Write: 0x70 Read: 0x71) | Sec ACE U3200 (Write: 0x7E Read: 0x7F) |
|---|---|---|---|
| I2C_TBT_X_SCL | | I2C_TBT_X_SCL | I2C_TBT_X_SCL |
| I2C_TBT_X_SDA | | I2C_TBT_X_SDA | I2C_TBT_X_SDA |
| I2C_TBT_XA_INT_L | | I2C_TBT_XA_INT_L | I2C_TBT_XB_INT_L |
| I2C_TBT_XB_INT_L | | | |

## Ridge PCIE Caps

| | | |
|---|---|---|
| PCIE_TBT_X_R2D_C_P<0> | C3040 0.22UF | PCIE_TBT_X_R2D_P<0> |
| PCIE_TBT_X_R2D_C_N<0> | C3041 0.22UF | PCIE_TBT_X_R2D_N<0> |
| PCIE_TBT_X_R2D_C_P<1> | C3042 0.22UF | PCIE_TBT_X_R2D_P<1> |
| PCIE_TBT_X_R2D_C_N<1> | C3043 0.22UF | PCIE_TBT_X_R2D_N<1> |
| PCIE_TBT_X_R2D_C_P<2> | C3044 0.22UF | PCIE_TBT_X_R2D_P<2> |
| PCIE_TBT_X_R2D_C_N<2> | C3045 0.22UF | PCIE_TBT_X_R2D_N<2> |
| PCIE_TBT_X_R2D_C_P<3> | C3046 0.22UF | PCIE_TBT_X_R2D_P<3> |
| PCIE_TBT_X_R2D_C_N<3> | C3047 0.22UF | PCIE_TBT_X_R2D_N<3> |
| PCIE_TBT_X_D2R_C_P<0> | C3050 0.22UF | PCIE_TBT_X_D2R_P<0> |
| PCIE_TBT_X_D2R_C_N<0> | C3051 0.22UF | PCIE_TBT_X_D2R_N<0> |
| PCIE_TBT_X_D2R_C_P<1> | C3052 0.22UF | PCIE_TBT_X_D2R_P<1> |
| PCIE_TBT_X_D2R_C_N<1> | C3053 0.22UF | PCIE_TBT_X_D2R_N<1> |
| PCIE_TBT_X_D2R_C_P<2> | C3054 0.22UF | PCIE_TBT_X_D2R_P<2> |
| PCIE_TBT_X_D2R_C_N<2> | C3055 0.22UF | PCIE_TBT_X_D2R_N<2> |
| PCIE_TBT_X_D2R_C_P<3> | C3056 0.22UF | PCIE_TBT_X_D2R_P<3> |
| PCIE_TBT_X_D2R_C_N<3> | C3057 0.22UF | PCIE_TBT_X_D2R_N<3> |

BOM_COST_GROUP=TBT

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|---|---|
| PAGE TITLE | USB-C X Support |
| Apple Inc. | |
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
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| PAGE | 30 OF 200 |
| SHEET | 29 OF 131 |

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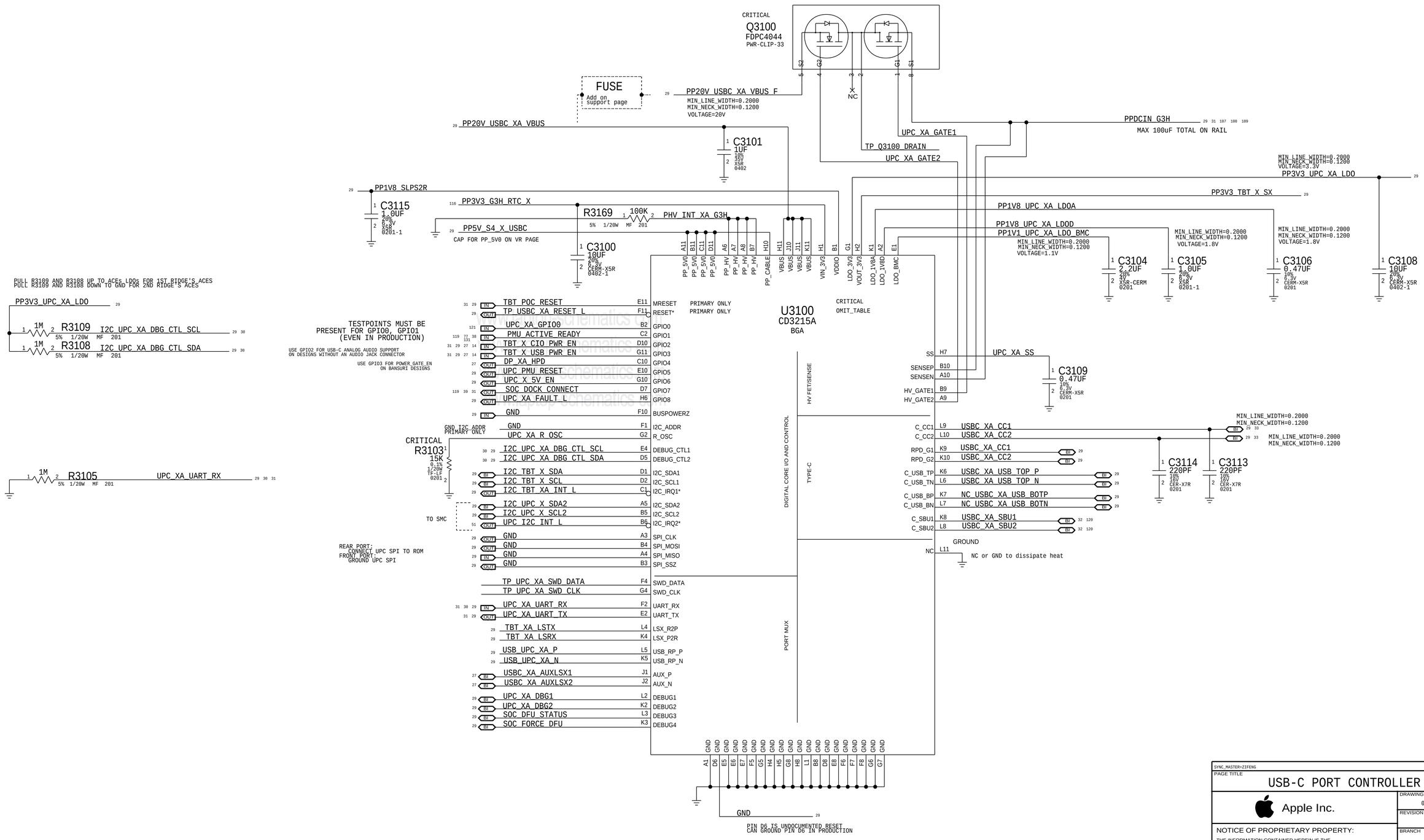
# PRIMARY ACE USB-C PORT CONTROLLER (UPC)

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SYNC_MASTER=ZIFENG SYNC_DATE=05/26/2017

PAGE TITLE

USB-C PORT CONTROLLER A

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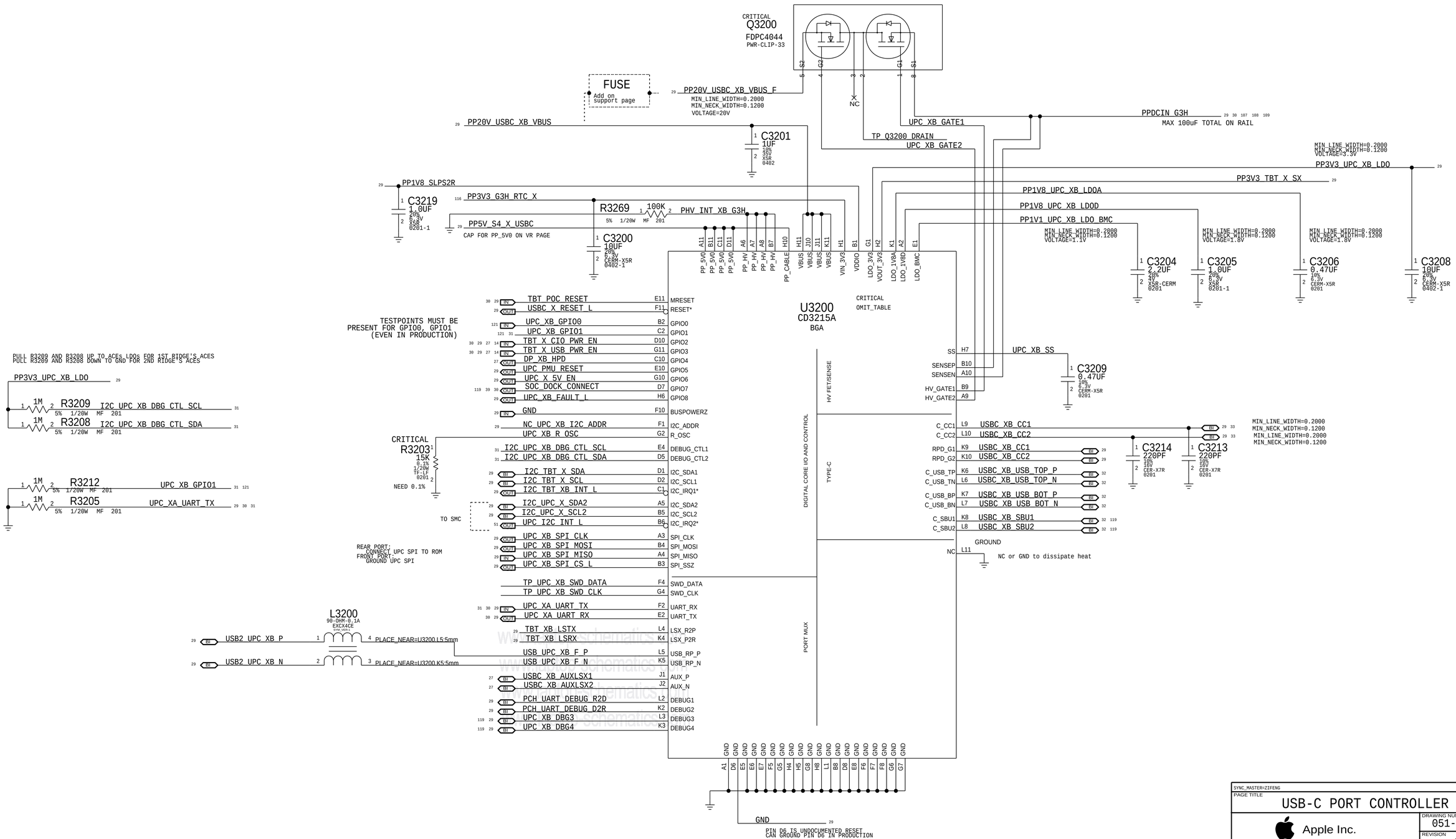
| SIZE | D |
| REVISION | 1.0.0 |
| BRANCH | EVT |
| PAGE | 31 OF 200 |
| SHEET | 30 OF 131 |

# SECONDARY ACE USB-C PORT CONTROLLER (UPC)

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SYNC_MASTER=ZIFENG SYNC_DATE=05/26/2017

PAGE TITLE
USB-C PORT CONTROLLER B

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 32 OF 200
SHEET 31 OF 131

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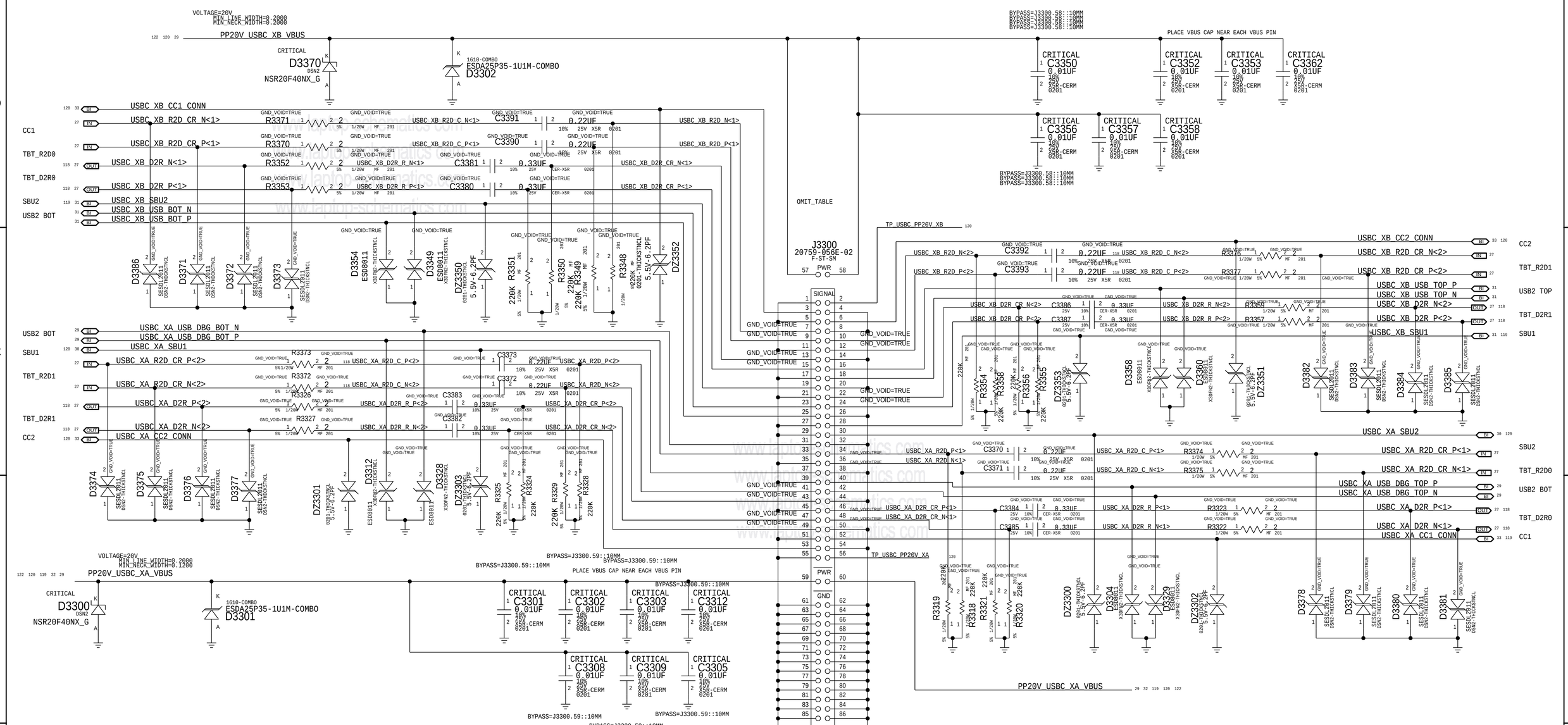


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PAGE TITLE
USB-C CONNECTOR A

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DRAWING NUMBER 051-02888 SIZE D

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PAGE 33 OF 200

SHEET 32 OF 131

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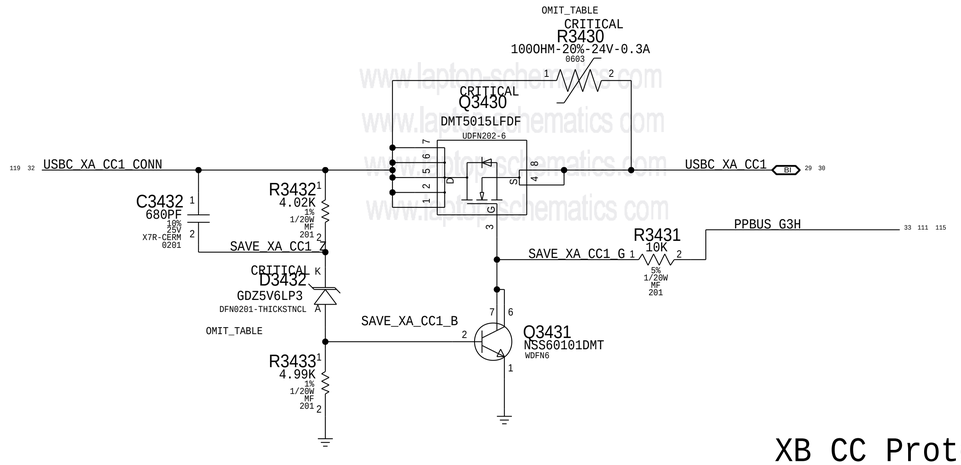
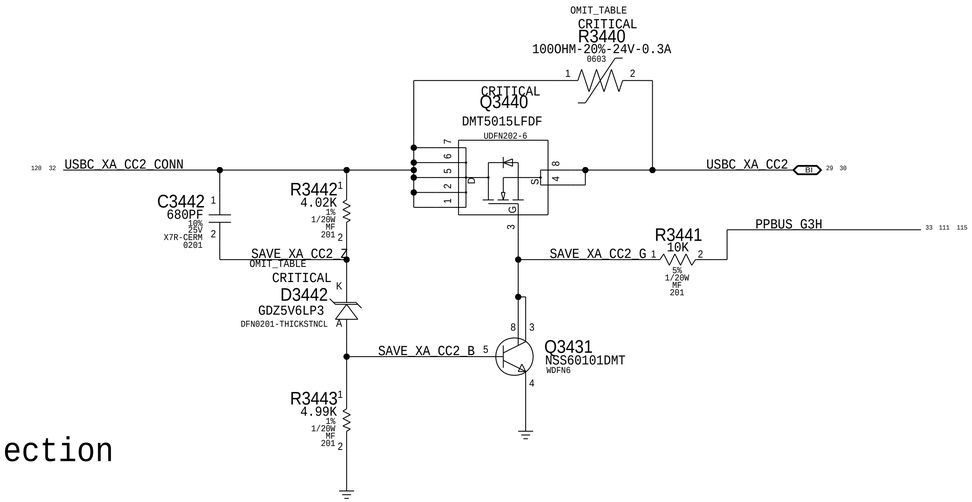
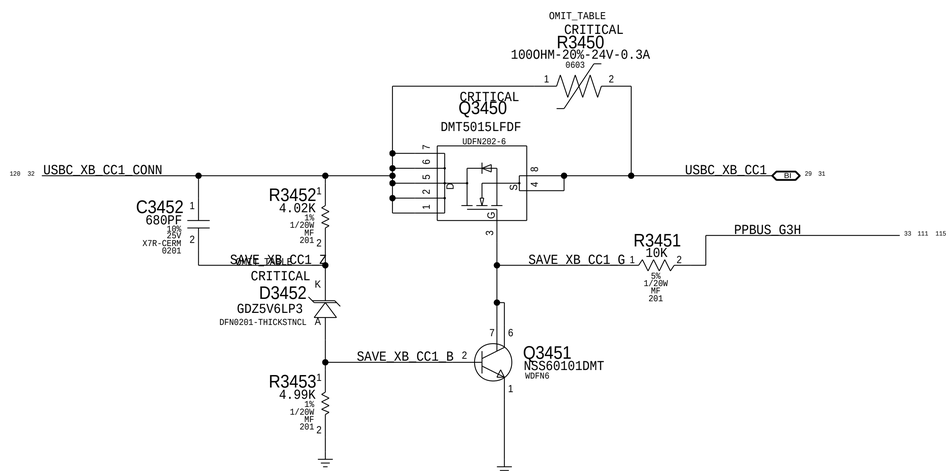
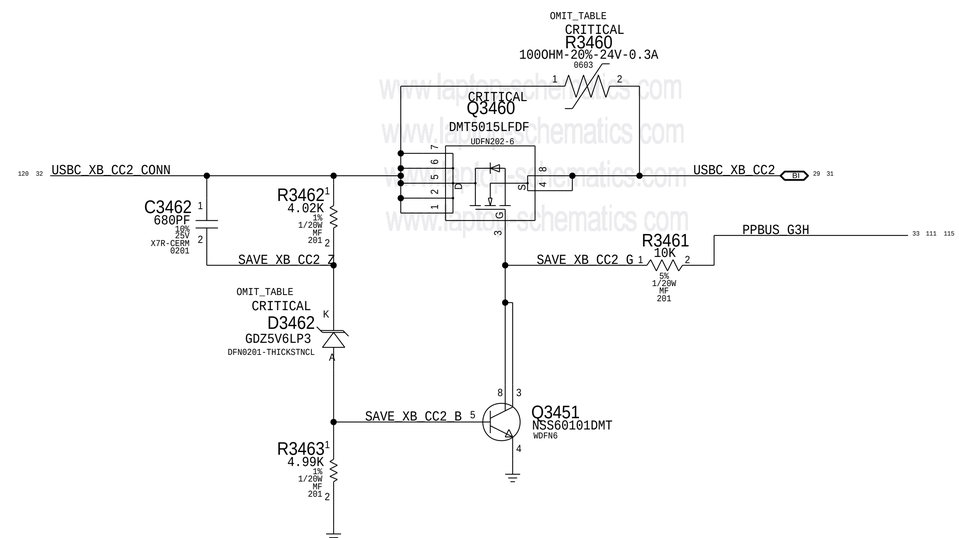
# XA CC Protection




# XB CC Protection




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 371S00181 | 4 | DIODE,ZENER,5.6V,250MW,DFN0201 | D3432,D3442,D3452,D3462 | CRITICAL | |
| 740S00050 | 4 | FUSE,THRMSTR,PTC,470OHM,24V,60MA,0603 | R3430,R3440,R3450,R3460 | CRITICAL | |

BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC X Connector Support

Apple Inc.

DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 34 OF 200
SHEET 33 OF 131

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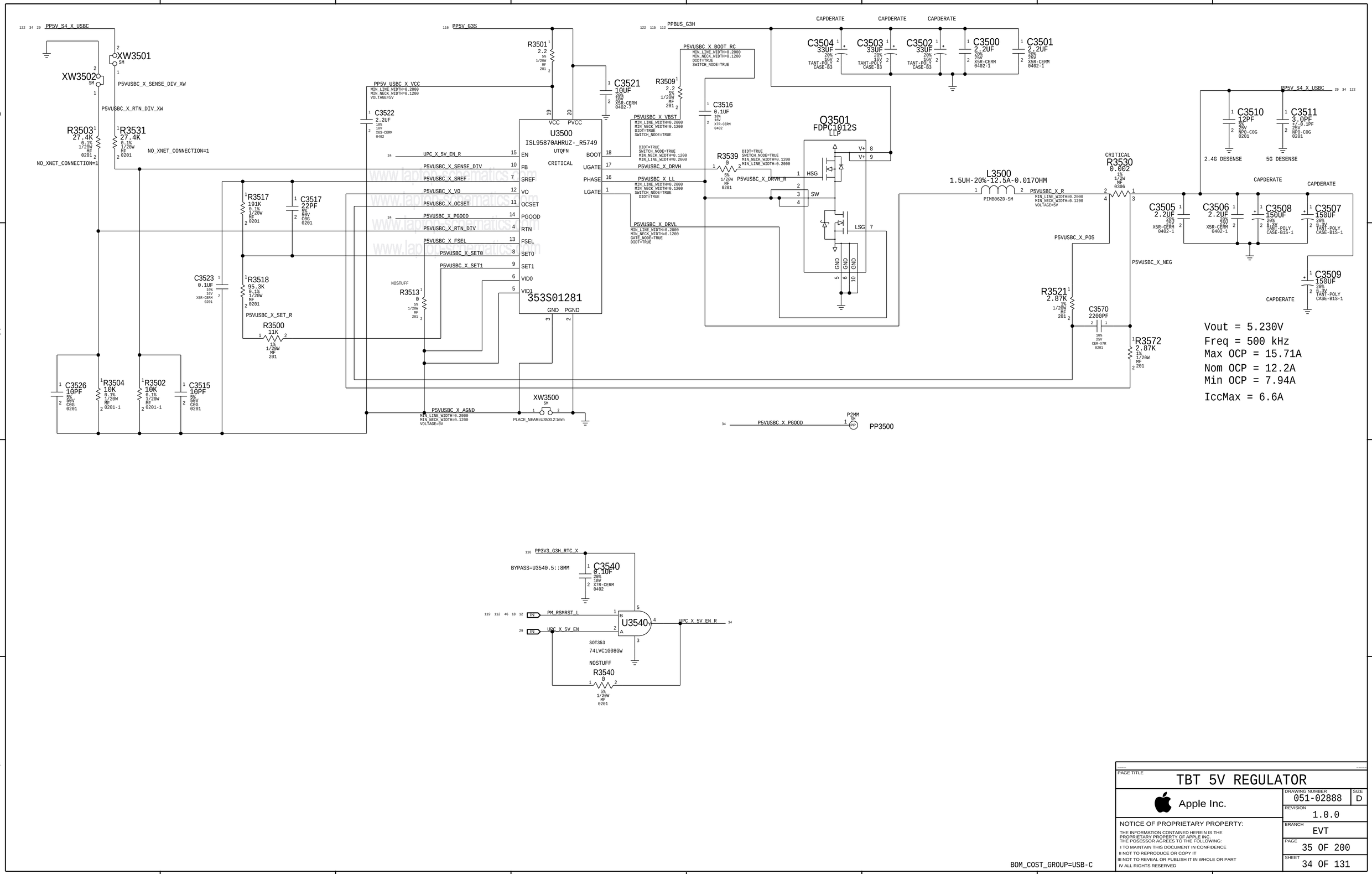


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PAGE TITLE

# TBT 5V REGULATOR

Apple Inc.

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PAGE 35 OF 200

SHEET 34 OF 131

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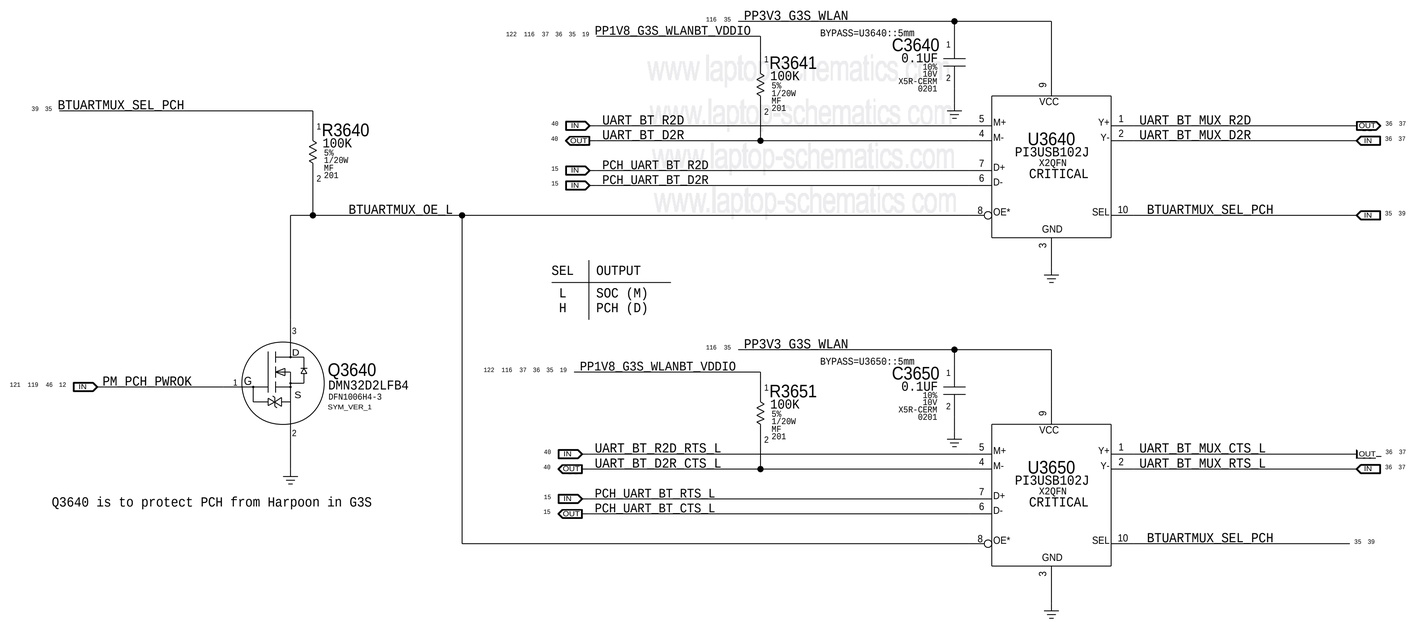


BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J132 SYNC_DATE=03/29/2017

PAGE TITLE

# WIFI/BT: Support

Apple Inc.

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REVISION 1.0.0

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PAGE 36 OF 200

SHEET 35 OF 131

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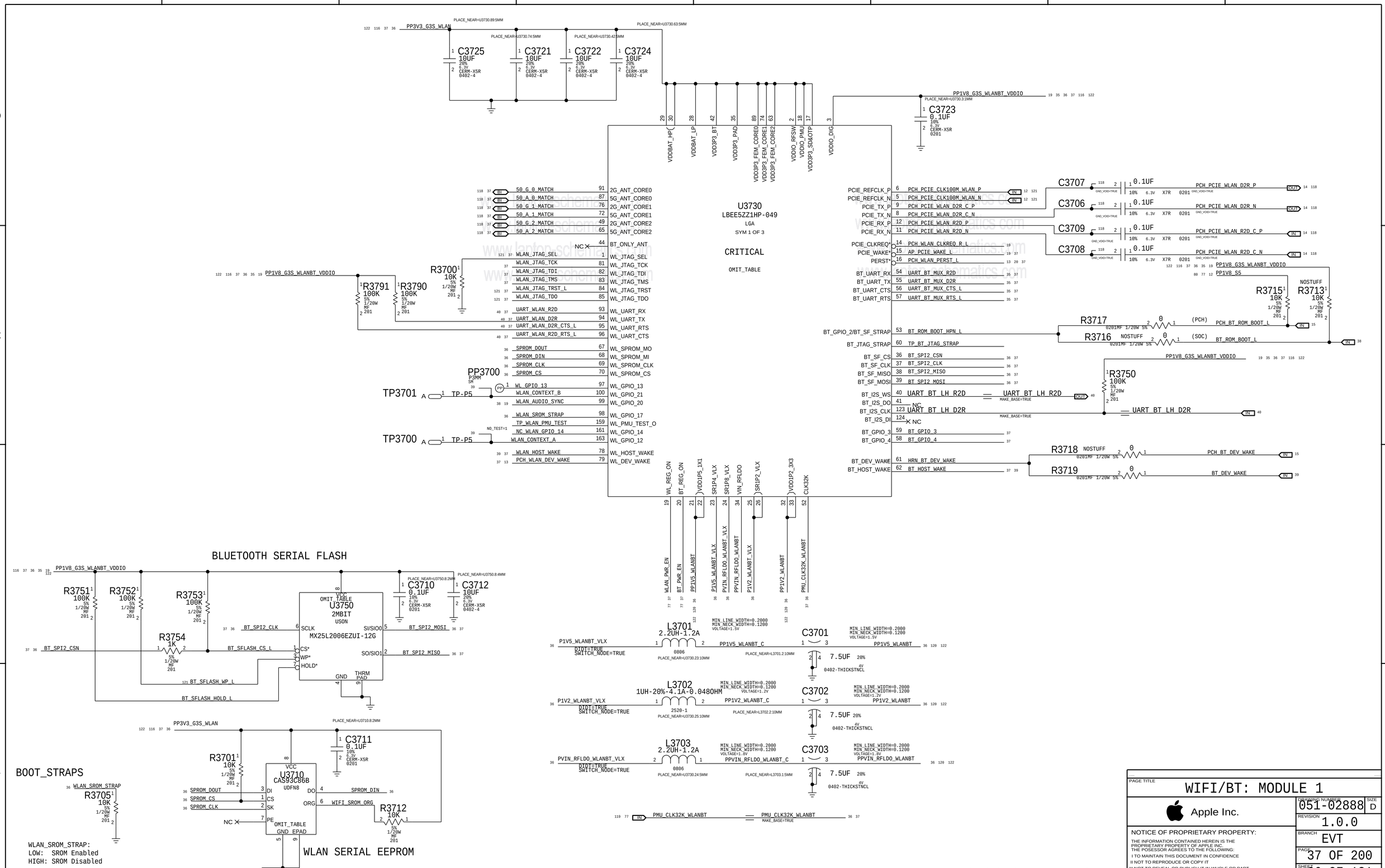


PAGE TITLE
# WIFI/BT: MODULE 1

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 37 OF 200
SHEET 36 OF 131

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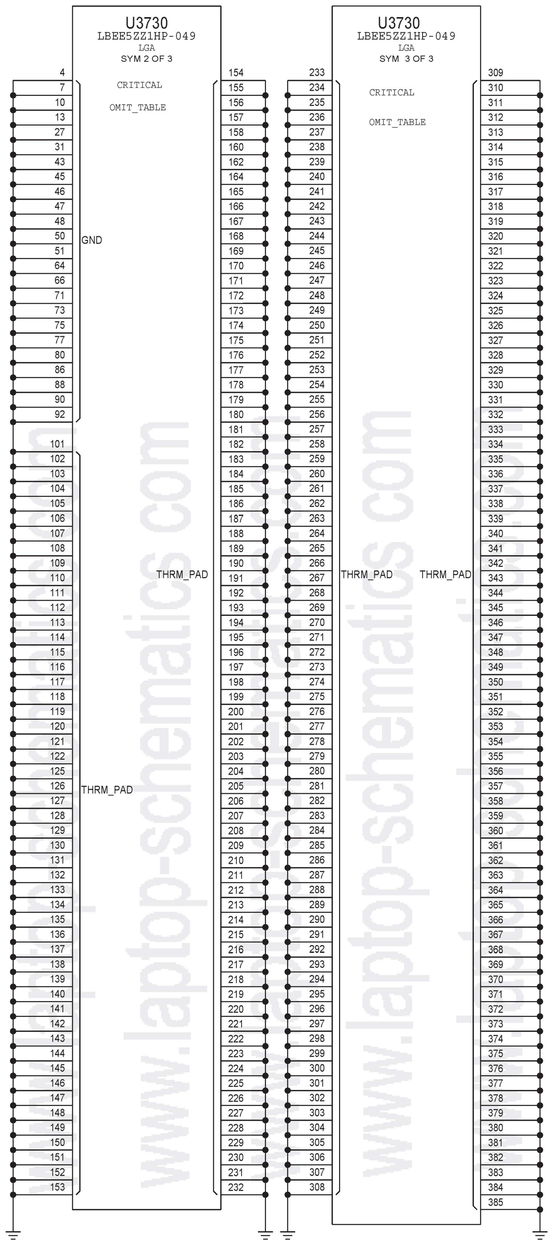
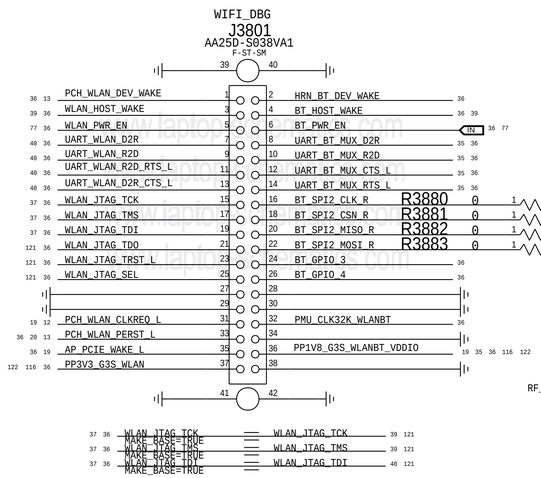
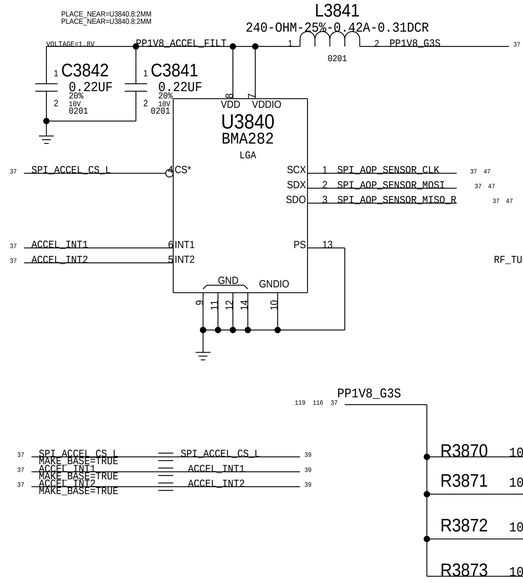
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 155S00196 | 2 | FILTER,DIPLEXER,LB/HB,LGA6 | U3810,U3830 | CRITICAL | RF_TUNING |



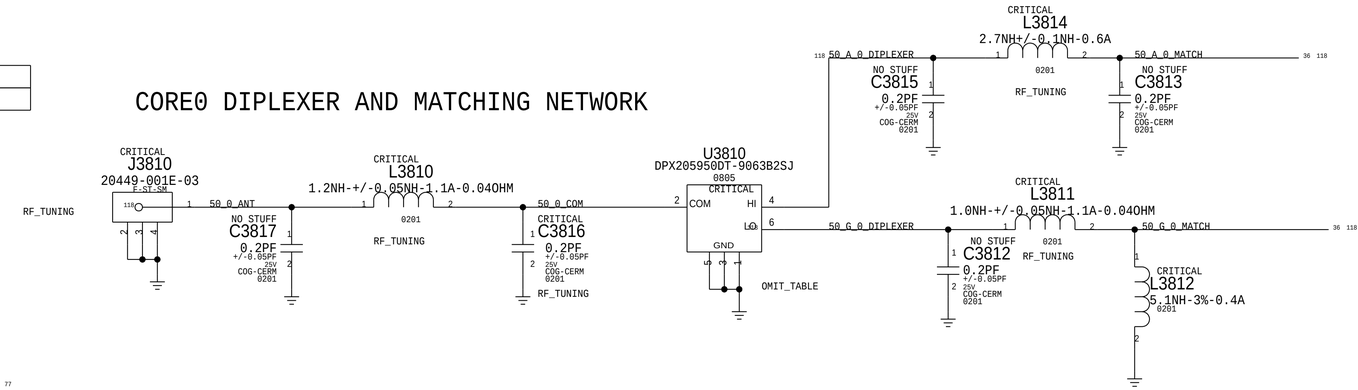

## DEBUG CONNECTOR



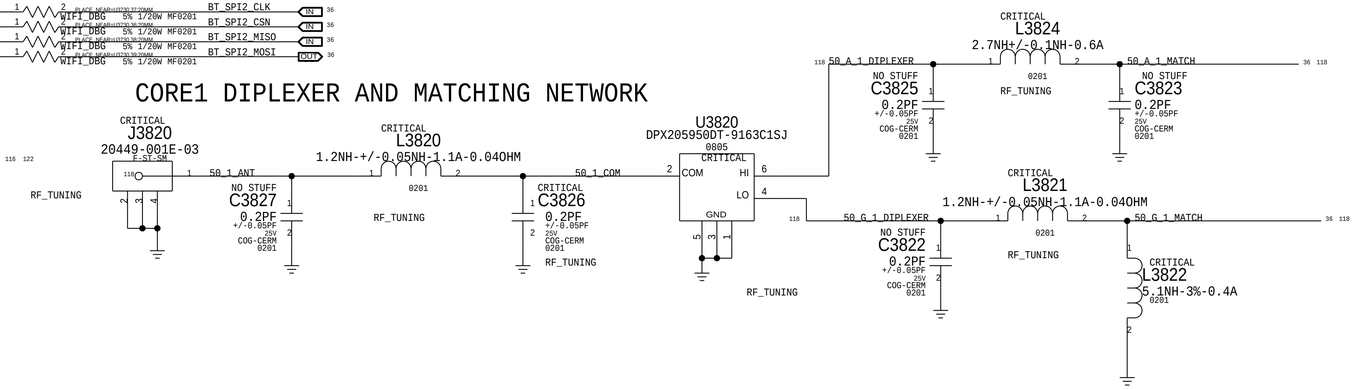

## ACCELERATION SENSOR



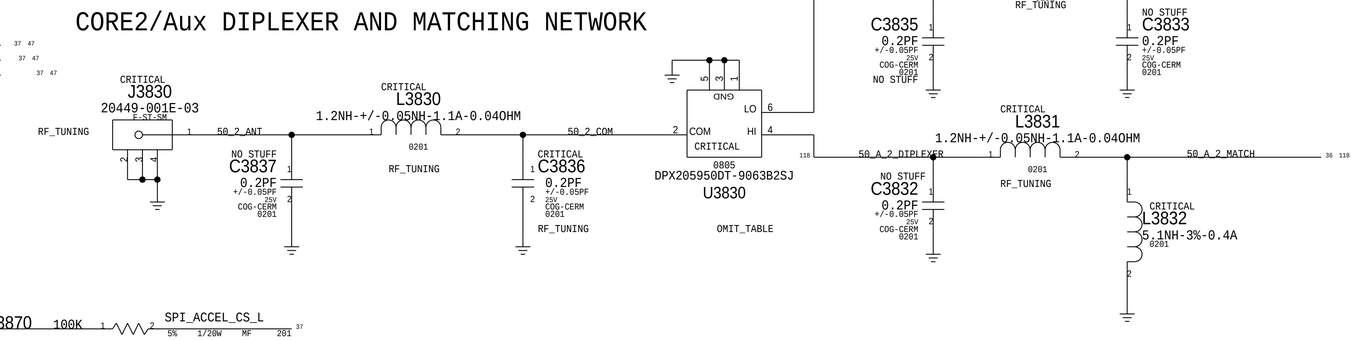

## CORE0 DIPLEXER AND MATCHING NETWORK




## CORE1 DIPLEXER AND MATCHING NETWORK




## CORE2/Aux DIPLEXER AND MATCHING NETWORK




BOM_COST_GROUP=WIRELESS

| | |
|---|---|
| PAGE TITLE | AP & BT Conn |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
| | REVISION 1.0.0 |
| | BRANCH EVT |
| | PAGE 38 OF 200 |
| | SHEET 37 OF 131 |

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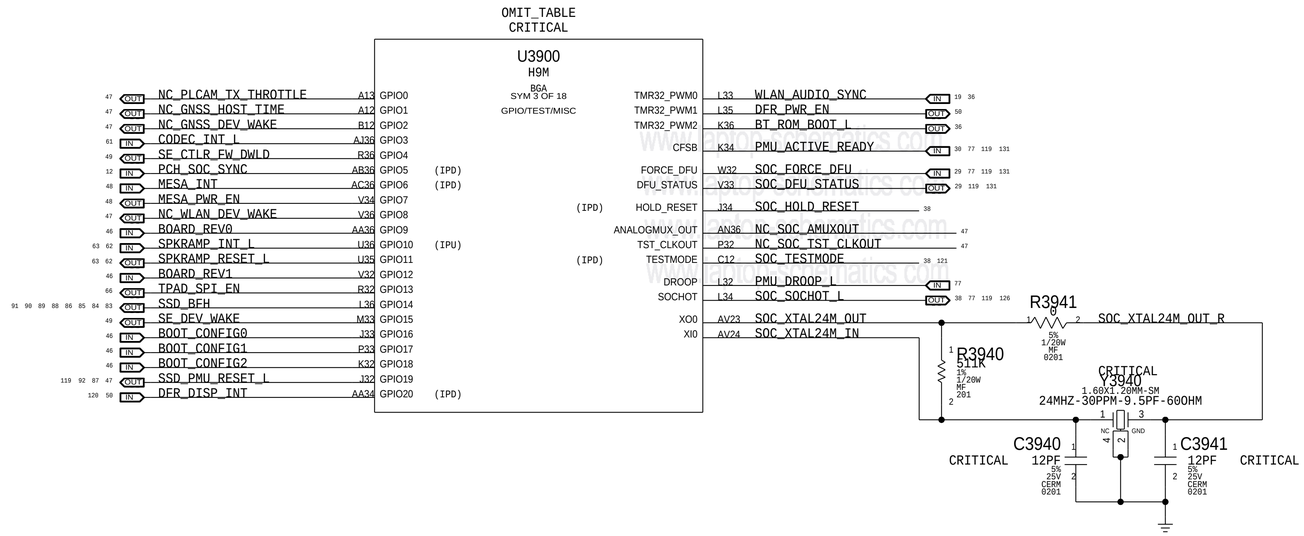
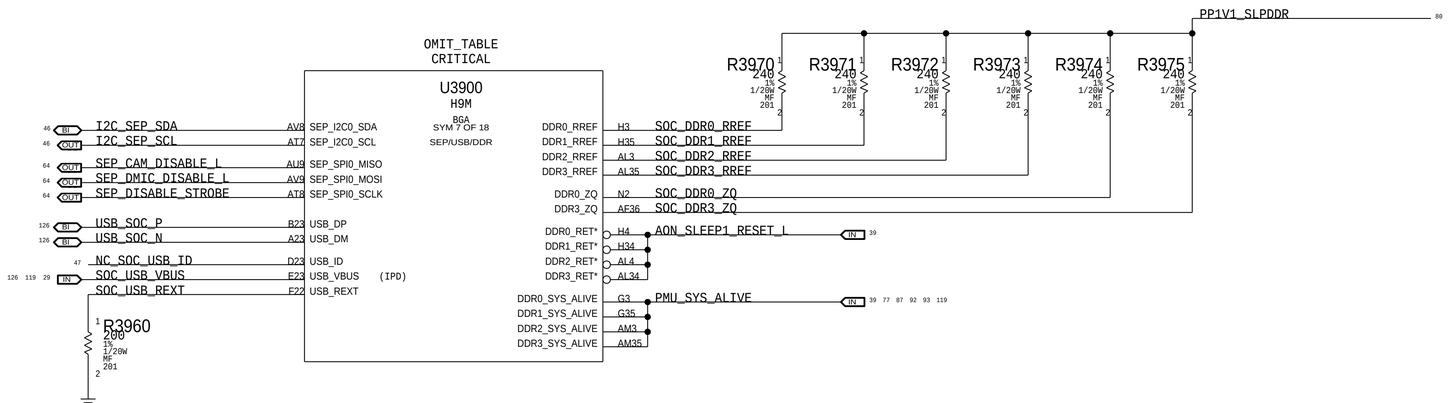
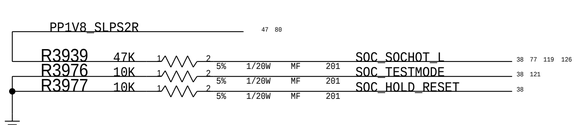
Note 1) IPU represents SW configured state, not HW default




BOM_COST_GROUP=SOC

SYNC_MASTER=S1LU SYNC_DATE=05/26/2017

PAGE TITLE
SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 39 OF 200
SHEET 38 OF 131

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OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 6 OF 18
AOP

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 36 | OUT | WLAN_CONTEXT_A | D3 | AOP_FUNC[0] | | AOP_PDM_CLK0 | P6 | PDM_DMIC_CLK0_R |
| 36 | OUT | WLAN_CONTEXT_B | F4 | AOP_FUNC[1] | | AOP_PDM_CLK1 | K2 | PDM_DMIC_CLK1_R |
| 37 | IN | ACCEL_INT1 | M6 | AOP_FUNC[2] | (IPD) | AOP_PDM_CLK2 (IPU) | J6 | SMC_FIXTURE_MODE_L |
| 37 | IN | ACCEL_INT2 | D4 | AOP_FUNC[3] | (IPD) | AOP_PDM_CLK3 (IPU) | L6 | NC_PLCAM_PROX_INT_L |
| 35 | OUT | BTUARTMUX_SEL_PCH | F3 | AOP_FUNC[4] | | AOP_PDM_CLK4 (IPU) | L5 | NC_PLCAM_ROMEO_B2B_DETECT |
| 20 15 | IN | SOC_PERST_L | K6 | AOP_FUNC[5] | | | | |
| 47 | IN | NC_ALTIMETER_INT | E4 | AOP_FUNC[6] | (IPD) | AOP_PDM_DATA0 (IPD) | J5 | PDM_DMIC_DATA0 |
| 37 | OUT | SPI_ACCEL_CS_L | J3 | AOP_FUNC[7] | | AOP_PDM_DATA1 (IPD) | K4 | PDM_DMIC_DATA1 |
| 47 | OUT | NC_SPI_ALTIMETER_CS_L | H6 | AOP_FUNC[8] | | | | |
| | | | | | | AOP_SPI_MOSI | D2 | SPI_AOP_SENSOR_MOSI_R |
| 47 | OUT | NC_I2C_AOP_SCL | N6 | AOP_I2C0_SCL | | AOP_SPI_SCLK | F2 | SPI_AOP_SENSOR_CLK_R |
| 47 | BI | NC_I2C_AOP_SDA | G5 | AOP_I2C0_SDA | | AOP_SPI_MISO | E2 | SPI_AOP_SENSOR_MISO |

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 5 OF 18
AON

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 120 50 | IN | DFR_TOUCH_INT_L | AL6 | AON_GPIO0 | | JTAG_TCK (IPU) | AK6 | SWD_SOC_SWCLK |
| 46 | IN | CPU_SMC_THRMTRIP_L | AE6 | AON_GPIO1 (IPU) | | JTAG_TMS (IPU) | AN5 | SWD_SOC_SWDIO |
| 117 | IN | GFX_SELF_THROTTLE_1V8 | AT5 | AON_GPIO2 (IPD) | | JTAG_TDI (IPU) | AH6 | DEBUG_JTAG_SOC_TDI |
| 47 | OUT | SMC_GPU_THRMTRIP | AN4 | AON_GPIO3 | | JTAG_TDO | AP4 | DEBUG_JTAG_SOC_TDO |
| 18 | IN | XDP_PRESENT_L | AK4 | AON_GPIO4 | | JTAG_TRST* (IPD) | AJ6 | TP_JTAG_SOC_TRST_L |
| 61 | OUT | CODEC_RESET_L | AV5 | AON_GPIO5 | | JTAG_SEL | AC6 | SOC_JTAG_SEL (DAP=0, TAP=1) |
| 36 | OUT | BT_DEV_WAKE | AR3 | AON_GPIO6 | | | | |
| 47 | IN | NC_PCIEDN_WAKE_L | AG6 | AON_GPIO7 (IPU) | | DOCK_CONNECT | AN2 | SOC_DOCK_CONNECT |
| 47 | OUT | NC_ENET_LOW_PWR | AU5 | AON_GPIO8 | | | | |
| 47 | IN | TPAD_SPI_INT_L | AP2 | AON_GPIO9 | | AON_SWD0_TMS | AJ4 | WLAN_JTAG_TMS |
| 47 | IN | NC_SDCONN_STATE_CHANGE_L | AR4 | AON_GPIO10 (IPU) | | AON_SWD1_TMS (IPU) | AH4 | NC_MESA_MENUKEY_L |
| 47 | IN | NC_ENET_MEDIA_SENSE | AN3 | AON_GPIO11 (IPD) | | AON_SWD01_TCK | AJ2 | WLAN_JTAG_TCK |
| 77 | IN | PMU_INT_L | AT6 | AON_GPIO12 (IPU) | | WDOG | AJ5 | SOC_WDOG |
| | | | | | | AON_SLEEP1_RESET* | AF6 | AON_SLEEP1_RESET_L |
| | | | | AON_SPMI_SCLK | | | | |
| | | | | AON_SPMI_SDATA | | | | |
| 119 77 | IN | PMU_CLK32K_SOC | AR5 | RT_CLK32768 | | | | |
| | | | AK2 | COLD_RESET* | | | | |
| | | | AK3 | CFSB_AON | | | | |
| 121 119 77 64 | IN | PMU_COLD_RESET_L | | | | | | |

PLACE_NEAR=U3900.AD6:5MM
PLACE_NEAR=U7800.M7:5MM

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 77 | OUT | SPMI_CLK | R4036 | 20 | 5% | 1/20W | MF | 201 |
| 77 | BI | SPMI_DATA | R4037 | 20 | 5% | 1/20W | MF | 201 |

R4039 4.7K 5% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 9 OF 18
SMC

PLACE_NEAR=U3900.U2:5MM
PLACE_NEAR=U3900.V2:5MM
PLACE_NEAR=U3900.U3:5MM
PLACE_NEAR=U3900.V4:5MM

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 118 39 20 12 | BI | ESPI_IO<0> | R4050 | 20 | 5% | 1/20W | MF | 201 |
| 118 39 20 12 | BI | ESPI_IO<1> | R4051 | 20 | 5% | 1/20W | MF | 201 |
| 118 39 20 12 | BI | ESPI_IO<2> | R4052 | 20 | 5% | 1/20W | MF | 201 |
| 118 39 20 12 | BI | ESPI_IO<3> | R4053 | 20 | 5% | 1/20W | MF | 201 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | ESPI_IO_R<0> | V2 | SMC_ESPI_IO0 | | SMC_GPIO0 | Y4 | CODEC_WAKE_L |
| | | ESPI_IO_R<1> | U3 | SMC_ESPI_IO1 | | SMC_GPIO1 (IPD) | Y8 | BT_HOST_WAKE |
| | | ESPI_IO_R<2> | U4 | SMC_ESPI_IO2 | | SMC_GPIO2 (IPD) | Y5 | WLAN_HOST_WAKE |
| | | ESPI_IO_R<3> | V8 | SMC_ESPI_IO3 | | SMC_GPIO3 | AA2 | GFX_THROTTLE_1V8_L |
| 20 | IN | ESPI_CLK60M | U2 | SMC_ESPI_CLK | (IPD) | SMC_GPIO4 | Y7 | LID_OPEN_RIGHT |
| 39 20 12 | IN | ESPI_CS_L | V6 | SMC_ESPI_CS* | | SMC_GPIO5 (IPD) | Y6 | PCC_EVENT |
| 119 20 12 | IN | ESPI_RESET_L | V5 | SMC_ESPI_RESET* | (IPD) | SMC_GPIO6 | AB2 | NC_TPAD_VIBE_L |
| | | | | | | SMC_GPIO7 | AD5 | TPAD_KBD_WAKE_L |
| 46 | IN | SMC_PECI_RX | M5 | SMC_PECI_IN | (IPD) | SMC_GPIO8 | AD2 | LID_OPEN_LEFT |
| 46 | OUT | SMC_PECI_TX | T6 | SMC_PECI_OUT | | SMC_GPIO9 | AB4 | NC_SPI_DSCRPTR_OVERRIDE_L |
| 121 46 | OUT | SMC_PCH_PWROK | W7 | PCH_PWROK | | SMC_GPIO10 (IPU) | AC2 | DISP_GCON_INT_L |
| 121 46 | OUT | SMC_PCH_SYS_PWROK | W8 | SYS_PWROK | | SMC_GPIO11 | AC3 | PCH_GCON_INT_L |
| | | | | | | SMC_GPIO12 | AA8 | TPAD_ACTUATOR_DISABLE_L |
| 46 | OUT | SMC_RSMRST_L | W6 | RSMRST* | | SMC_GPIO13 (IPU) | AB3 | TBT_WAKE_L |
| 121 119 46 | OUT | SMC_SYSRST_L | W4 | SYS_RESET* | | SMC_GPIO14 (IPU) | AE2 | UPC_I2C_INT_L |
| 131 119 77 12 | IN | PM_SLP_S0_L | AA4 | SLP_S0B | | SMC_GPIO15 (IPD) | L4 | NC_GNSS_HOST_WAKE |
| 69 47 46 | BI | SMC_PROCHOT_L | R5 | PROCHOT* | | | | |
| 119 93 92 87 77 38 | IN | PMU_SYS_ALIVE | AA6 | SYS_ALIVE | | SMC_ADC0 | AG2 | SMC_DCIN_VSENSE |
| | | | | | | SMC_ADC1 | AC4 | SMC_DCIN_ISENSE |
| 119 51 | OUT | I2C_UPC_SCL | M3 | SMC_I2C0_SCL | | SMC_ADC2 | AH3 | SMC_PBUS_VSENSE |
| 119 51 | BI | I2C_UPC_SDA | J4 | SMC_I2C0_SDA | | SMC_ADC3 | AD4 | SMC_BMON_ISENSE |
| 51 | OUT | I2C_SNS0_S0_SCL | N4 | SMC_I2C1_SCL | | SMC_ADC4 | AB6 | SMC_CPU_HI_ISENSE |
| 51 | BI | I2C_SNS0_S0_SDA | P4 | SMC_I2C1_SDA | | SMC_ADC5 | AH2 | SMC_GPU_HS_ISENSE |
| | | | | | | SMC_ADC6 | AG4 | SMC_P3V3_WLAN_ISENSE |
| 51 | OUT | I2C_SNS1_S0_SCL | U5 | SMC_I2C2_SCL | | SMC_ADC7 | AC5 | SMC_P3V3_CAPLE_ISENSE |
| 51 | BI | I2C_SNS1_S0_SDA | M2 | SMC_I2C2_SDA | | REFP_ADC | AF4 | PP1V25_SLPS2R_SMC_AVREF 46 |
| | | | | | | REFM_ADC 58 | AG3 | GND_SMC_AVSS |
| 51 | OUT | I2C_DISP_SCL | U6 | SMC_I2C3_SCL | | | | |
| 51 | BI | I2C_DISP_SDA | R4 | SMC_I2C3_SDA | | SMC_PWM0 | J2 | SMC_FAN_0_PWM |
| | | | | | | SMC_TACH0 | L3 | SMC_FAN_0_TACH |
| 119 51 | OUT | I2C_PWR_SCL | P3 | SMC_I2C4_SCL | | | | |
| 119 51 | BI | I2C_PWR_SDA | T4 | SMC_I2C4_SDA | | SMC_PWM1 | R6 | SMC_FAN_1_PWM |
| | | | | | | SMC_TACH1 | L2 | SMC_FAN_1_TACH |
| 51 | OUT | I2C_SNS_G3S_SCL | R2 | SMC_I2C5_SCL | | | | |
| 51 | BI | I2C_SNS_G3S_SDA | P2 | SMC_I2C5_SDA | | SMC_PWM2 | M4 | NC_SMC_LED_ONEWIRE |
| 51 | OUT | I2C_SSD_SCL | R3 | SMC_I2C6_SCL | | SMC_UART0_RXD (IPU) | V4 | SMC_DEBUGPRT_RX |
| 51 | BI | I2C_SSD_SDA | T2 | SMC_I2C6_SDA | | SMC_UART0_TXD | V5 | SMC_DEBUGPRT_TX |
| | | | | | | SWD_OUT0_TCK | AE3 | SSD0_SWCLK_UART_R2D |
| | | | | | | SWD_OUT0_TMS | AA5 | SSD0_SWDIO_UART_D2R |
| | | | | | | SWD_OUT1_TCK | AF2 | SSD1_SWCLK_UART_R2D |
| | | | | | | SWD_OUT1_TMS | AA7 | SSD1_SWDIO_UART_D2R |

XW4089
SM
PLACE_NEAR=U3900.AF3:4MM

PP1V8_S5 80

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| R4046 | 10K | 5% | 1/20W | MF | 201 | SOC_JTAG_SEL | 39 121 |
| R4047 | 100K | 5% | 1/20W | MF | 201 | SOC_DOCK_CONNECT | 30 31 39 119 |
| R4054 | 100K | 5% | 1/20W | MF | 201 | ESPI_IO<0> | 12 20 39 118 |
| R4055 | 100K | 5% | 1/20W | MF | 201 | ESPI_IO<1> | 12 20 39 118 |
| R4056 | 100K | 5% | 1/20W | MF | 201 | ESPI_IO<2> | 12 20 39 118 |
| R4057 | 100K | 5% | 1/20W | MF | 201 | ESPI_IO<3> | 12 20 39 118 |
| R4059 | 100K | 5% | 1/20W | MF | 201 | ESPI_CS_L | 12 20 39 |

BOM_COST_GROUP=SOC

SYNC_MASTER=SILU SYNC_DATE=03/22/2017

PAGE TITLE
SoC AOP/AON/SMC

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 40 OF 200
SHEET 39 OF 131

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OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 4 OF 18
ISP

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 82 47 | IN | MIPI_FTCAM_DATA_P<0> | B27 | MIPI0C_DATA0_P | | | |
| 82 47 | IN | MIPI_FTCAM_DATA_N<0> | A27 | MIPI0C_DATA0_N | | | |
| 47 | IN | GND | B25 | MIPI0C_DATA1_P | | | |
| 47 | IN | GND | A25 | MIPI0C_DATA1_N | | | |
| 82 47 | IN | MIPI_FTCAM_CLK_P | B26 | MIPI0C_CLK_P | | | |
| 82 47 | IN | MIPI_FTCAM_CLK_N | A26 | MIPI0C_CLK_N | | | |
| 47 | IN | GND | B28 | MIPI1C_DATA0_P | | | |
| 47 | IN | GND | A28 | MIPI1C_DATA0_N | | | |
| 47 | IN | GND | B30 | MIPI1C_DATA1_P | | | |
| 47 | IN | GND | A30 | MIPI1C_DATA1_N | | | |
| 47 | IN | GND | B29 | MIPI1C_CLK_P | | | |
| 47 | IN | GND | A29 | MIPI1C_CLK_N | | | |
| 50 | OUT | MIPI_DFR_DATA_P | B33 | MIPID_DATA0_P | | | |
| 50 | OUT | MIPI_DFR_DATA_N | A33 | MIPID_DATA0_N | | | |
| 50 | OUT | MIPI_DFR_CLK_P | B32 | MIPID_CLK_P | | | |
| 50 | OUT | MIPI_DFR_CLK_N | A32 | MIPID_CLK_N | | | |
| | | SOC_MIPI0C_REXT | F23 | MIPI0C_REXT | | | |
| | | SOC_MIPI1C_REXT | F26 | MIPI1C_REXT | | | |
| | | SOC_MIPID_REXT | F27 | MIPID_REXT | | | |
| | | | | | | ISP_I2C0_SDA | AF32 | I2C_FTCAM_SDA | BI 52 |
| | | | | | | ISP_I2C0_SCL | AH36 | I2C_FTCAM_SCL | OUT 52 |
| | | | | | | ISP_I2C1_SDA | AB32 | NC_I2C_PLCAM_SDA | BI 52 |
| | | | | | | ISP_I2C1_SCL | AG32 | NC_I2C_PLCAM_SCL | OUT 52 |
| | | | | | | SENSOR0_CLK | AK35 | NC_FTCAM_CLK12M_R | OUT 47 |
| | | | | | | SENSOR0_RST | AK34 | NC_FTCAM_RESET_L | OUT 47 |
| | | | | | | SENSOR0_ISTRB | AJ33 | DFR_TOUCH_RESET_L | OUT 50 120 |
| | | | | | | SENSOR1_CLK | AD33 | NC_PLCAM_RX_CLK12M_R | OUT 47 |
| | | | | | | SENSOR1_RST | AC32 | NC_PLCAM_RX_RESET_L | OUT 47 |
| | | | | | | SENSOR1_ISTRB | AC34 | DFR_DISP_RESET_L | OUT 50 120 |
| | | | | | | SENSOR2_CLK | AD32 | NC_PLCAM_TX_CLK12M_R | OUT 47 |
| | | | | | | SENSOR2_RST | AJ32 | NC_PLCAM_TX_RESET_L | OUT 47 |
| | | | | | (IPD) | SENSOR_INT | AA33 | NC_PLCAM_TX_INT | IN 47 |
| | | | | | (IPD) | DISP_TE | H32 | DFR_DISP_TE | IN 50 120 |
| | | | | | | DISP_VSYNC | T36 | BOARD_REV2 | IN 46 |
| | | | | | | CLK32K_OUT | AK33 | DFR_TOUCH_CLK32K_RESET_L | OUT 50 120 |

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 2 OF 18
I2C/UART/SPI/I2S

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 52 | BI | I2C_SPKRAMP_L_SDA | AE35 | I2C0_SDA | | | |
| 52 | OUT | I2C_SPKRAMP_L_SCL | AD35 | I2C0_SCL | | | |
| 52 | BI | I2C_SPKRAMP_R_SDA | AE34 | I2C1_SDA | | | |
| 52 | OUT | I2C_SPKRAMP_R_SCL | AG35 | I2C1_SCL | | | |
| 52 | BI | I2C_CODEC_SDA | M34 | I2C2_SDA | | | |
| 52 | OUT | I2C_CODEC_SCL | R33 | I2C2_SCL | | | |
| 120 52 | BI | I2C_ALS_SDA | Y32 | I2C3_SDA | | | |
| 120 52 | OUT | I2C_ALS_SCL | AE34 | I2C3_SCL | | | |
| 52 | BI | I2C_DFR_SDA | T34 | I2C4_SDA | | | |
| 52 | OUT | I2C_DFR_SCL | U32 | I2C4_SCL | | | |
| 52 | BI | NC_I2C_SOC_5_SDA | R35 | I2C5_SDA | | | |
| 52 | OUT | NC_I2C_SOC_5_SCL | U33 | I2C5_SCL | | | |
| 47 | IN | NC_SPKR_ID1 | P34 | I2C6_SDA | (IPU) | | |
| 120 63 | IN | SPKR_ID0 | R34 | I2C6_SCL | (IPU) | | |
| 126 119 | IN | SOC_DEBUGPRT_RX | Y33 | UART0_RXD | (IPU) | | |
| 126 119 | OUT | SOC_DEBUGPRT_TX | Y34 | UART0_TXD | | | |
| 49 | IN | UART_SE_D2R | B15 | UART1_RXD | | | |
| 49 | OUT | UART_SE_R2D | A15 | UART1_TXD | | | |
| 49 | IN | UART_SE_D2R_CTS_L | C15 | UART1_CTS* | | | |
| 49 | OUT | UART_SE_R2D_RTS_L | D15 | UART1_RTS* | | | |
| 35 | IN | UART_BT_D2R | J36 | UART2_RXD | | | |
| 35 | OUT | UART_BT_R2D | J35 | UART2_TXD | | | |
| 35 | IN | UART_BT_D2R_CTS_L | N38 | UART2_CTS* | | | |
| 35 | OUT | UART_BT_R2D_RTS_L | M38 | UART2_RTS* | | | |
| 36 | IN | UART_BT_LH_D2R | M36 | UART3_RXD | | | |
| 36 | OUT | UART_BT_LH_R2D | N36 | UART3_TXD | | | |
| 47 | IN | NC_UART_GNSS_D2R_CTS_L | M35 | UART3_CTS* | | | |
| 47 | OUT | NC_UART_GNSS_R2D_RTS_L | U34 | UART3_RTS* | | | |
| 37 36 | IN | UART_WLAN_D2R | B14 | UART4_RXD | | | |
| 37 36 | OUT | UART_WLAN_R2D | A14 | UART4_TXD | | | |
| 37 36 | IN | UART_WLAN_D2R_CTS_L | C14 | UART4_CTS* | | | |
| 37 36 | OUT | UART_WLAN_R2D_RTS_L | C13 | UART4_RTS* | | | |
| | | | | | | SPI0_MISO | AR9 | SPI_SOCROM_MISO | IN 46 |
| | | | | | | SPI0_MOSI | AR7 | SPI_SOCROM_MOSI_R | |
| | | | | | | SPI0_SCLK | AU7 | SPI_SOCROM_CLK_R | |
| | | | | | | SPI0_SSIN | AT9 | SPI_SOCROM_CS_L | OUT 46 |
| | | | | | (IPU) | SPI1_MISO | P36 | SPI_TPAD_MISO | IN 46 47 |
| | | | | | | SPI1_MOSI | N34 | SPI_TPAD_MOSI_R | OUT 47 |
| | | | | | | SPI1_SCLK | P35 | SPI_TPAD_CLK_R | OUT 47 |
| | | | | | | SPI1_SSIN | T32 | SPI_TPAD_CS_L | OUT 66 |
| | | | | | | SPI2_MISO | A19 | SPI_MESA_MISO | IN 48 |
| | | | | | | SPI2_MOSI | A20 | SPI_MESA_MOSI_R | OUT 47 |
| | | | | | | SPI2_SCLK | C19 | SPI_MESA_CLK_R | OUT 47 |
| | | | | | | SPI2_SSIN | A18 | WLAN_JTAG_TDI | OUT 37 121 |
| | | | | | | SPI3_MISO | C17 | SPI_DFR_MISO | IN 47 |
| | | | | | | SPI3_MOSI | C18 | SPI_DFR_MOSI_R | OUT 47 |
| | | | | | | SPI3_SCLK | B18 | SPI_DFR_CLK_R | OUT 47 |
| | | | | | | SPI3_SSIN | A17 | SPI_DFR_CS_L | OUT 50 120 |
| | | | | | (IPD) | I2S0_DIN | AC33 | I2S_SPKRAMP_L_D2R | IN 62 63 |
| | | | | | | I2S0_DOUT | AG34 | I2S_SPKRAMP_L_R2D_R | OUT 47 |
| | | | | | | I2S0_BCLK | AA32 | I2S_SPKRAMP_L_BCLK_R | OUT 47 |
| | | | | | | I2S0_LRCK | AG33 | I2S_SPKRAMP_L_LRCLK | OUT 47 |
| | | | | | | I2S0_MCK | AR35 | NC_DFR_TOUCH_RSVD | BI 47 |
| | | | | | (IPD) | I2S1_DIN | B20 | I2S_SPKRAMP_R_D2R | IN 47 |
| | | | | | | I2S1_DOUT | C20 | I2S_SPKRAMP_R_R2D_R | OUT 47 |
| | | | | | | I2S1_BCLK | C21 | I2S_SPKRAMP_R_BCLK_R | OUT 47 |
| | | | | | | I2S1_LRCK | A21 | I2S_SPKRAMP_R_LRCLK | OUT 47 |
| | | | | | | I2S1_MCK | D21 | NC_PCHROM_SW_EN | OUT 47 |
| | | | | | (IPD) | I2S2_DIN | AH34 | I2S_CODEC_D2R | IN 61 |
| | | | | | | I2S2_DOUT | AB34 | I2S_CODEC_R2D_R | OUT 47 |
| | | | | | | I2S2_BCLK | AF33 | I2S_CODEC_BCLK_R | OUT 47 |
| | | | | | | I2S2_LRCK | AH35 | I2S_CODEC_LRCLK | OUT 47 |
| | | | | | | I2S2_MCK | AR33 | NC_I2S_CODEC_MCLK | OUT 47 |
| | | | | | (IPD) | I2S3_DIN | AD36 | NC_I2S_HAWKING_D2R | IN 47 |
| | | | | | | I2S3_DOUT | AB35 | NC_I2S_CODEC1_R2D_R | OUT 47 |
| | | | | | | I2S3_BCLK | AE36 | NC_I2S_HAWKING_BCLK | OUT 47 |
| | | | | | | I2S3_LRCK | W34 | NC_I2S_HAWKING_LRCLK | OUT 47 |
| | | | | | | I2S3_MCK | AG36 | NC_I2S_CODEC1_MCLK | OUT 47 |

PLACE_NEAR=U3900.AR7:5MM
PLACE_NEAR=U3900.AU7:5MM

R4171 20 1 2 5% 1/20W MF 201 SPI_SOCROM_MOSI OUT 46
R4172 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CLK OUT 46

BOM_COST_GROUP=SOC

SYNC_MASTER=H9M and PMIC SYNC_DATE=03/02/2017

PAGE TITLE
SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 41 OF 200
SHEET 40 OF 131

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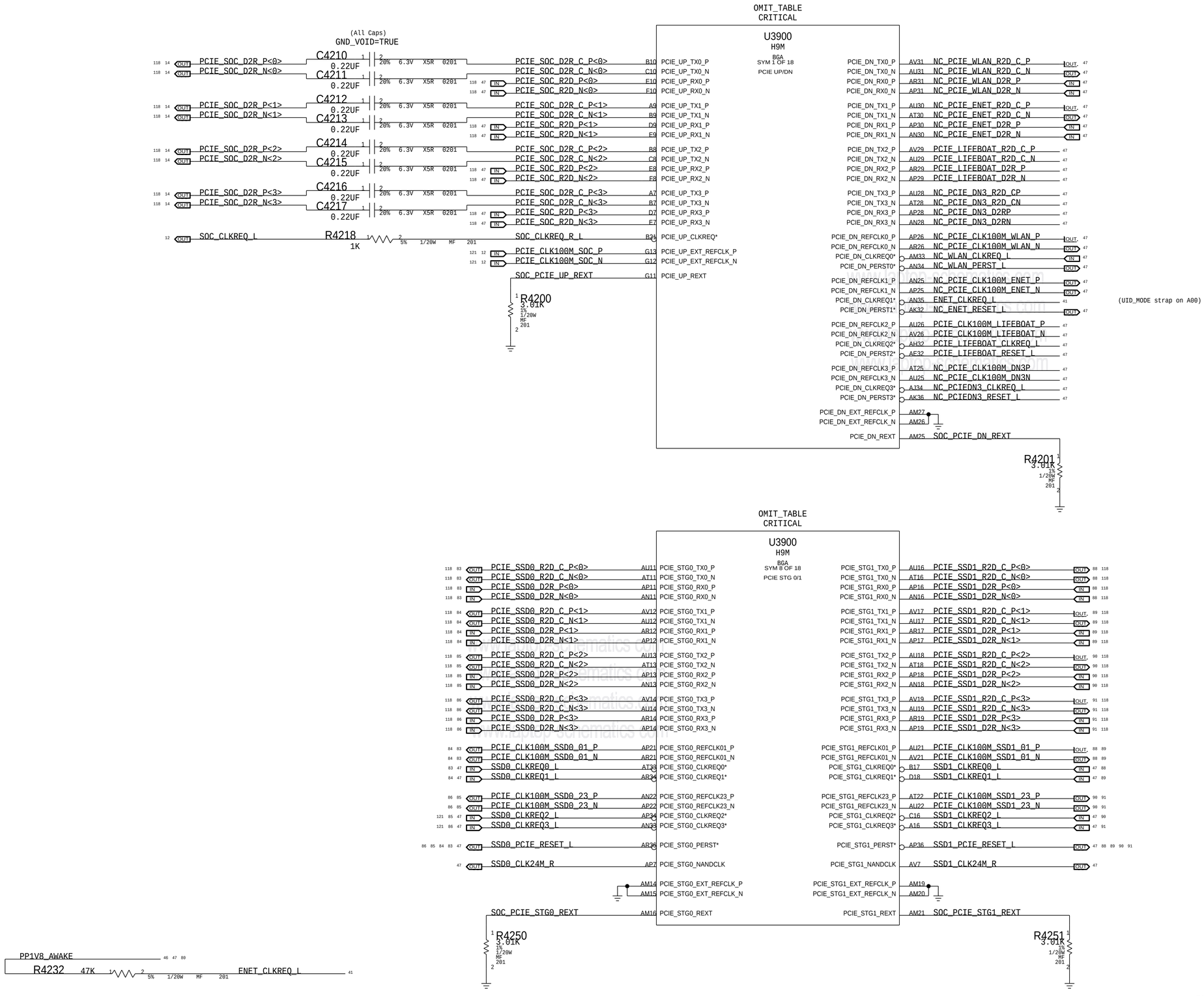


BOM_COST_GROUP=SOC

SYNC_MASTER=SILU SYNC_DATE=03/15/2017

PAGE TITLE

# SoC PCIe

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0

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PAGE 42 OF 200

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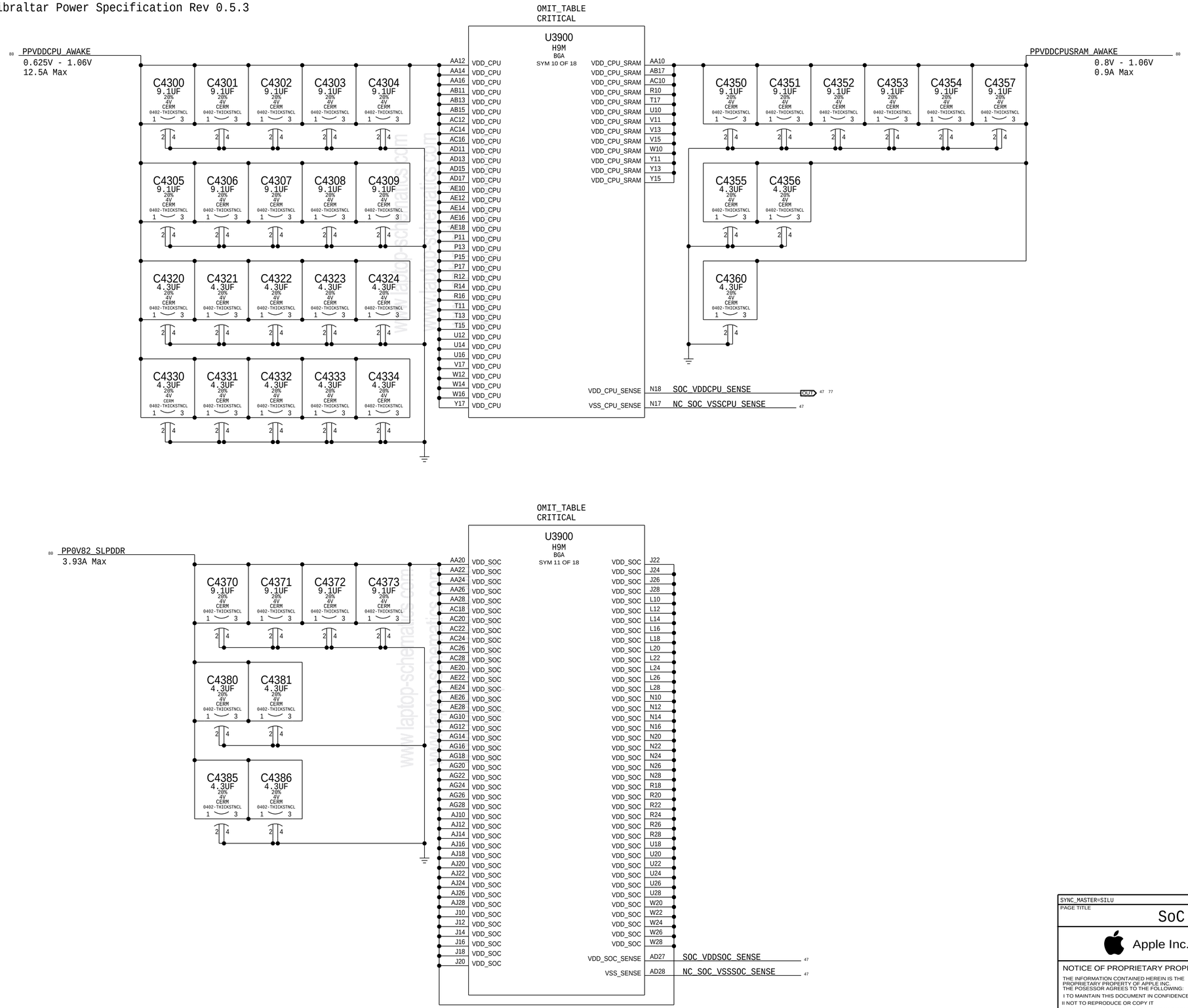
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

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| | |
|---|---|
| SYNC_MASTER=SILU | SYNC_DATE=04/04/2017 |
| PAGE TITLE | SoC Power 1 |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
| | REVISION 1.0.0 |
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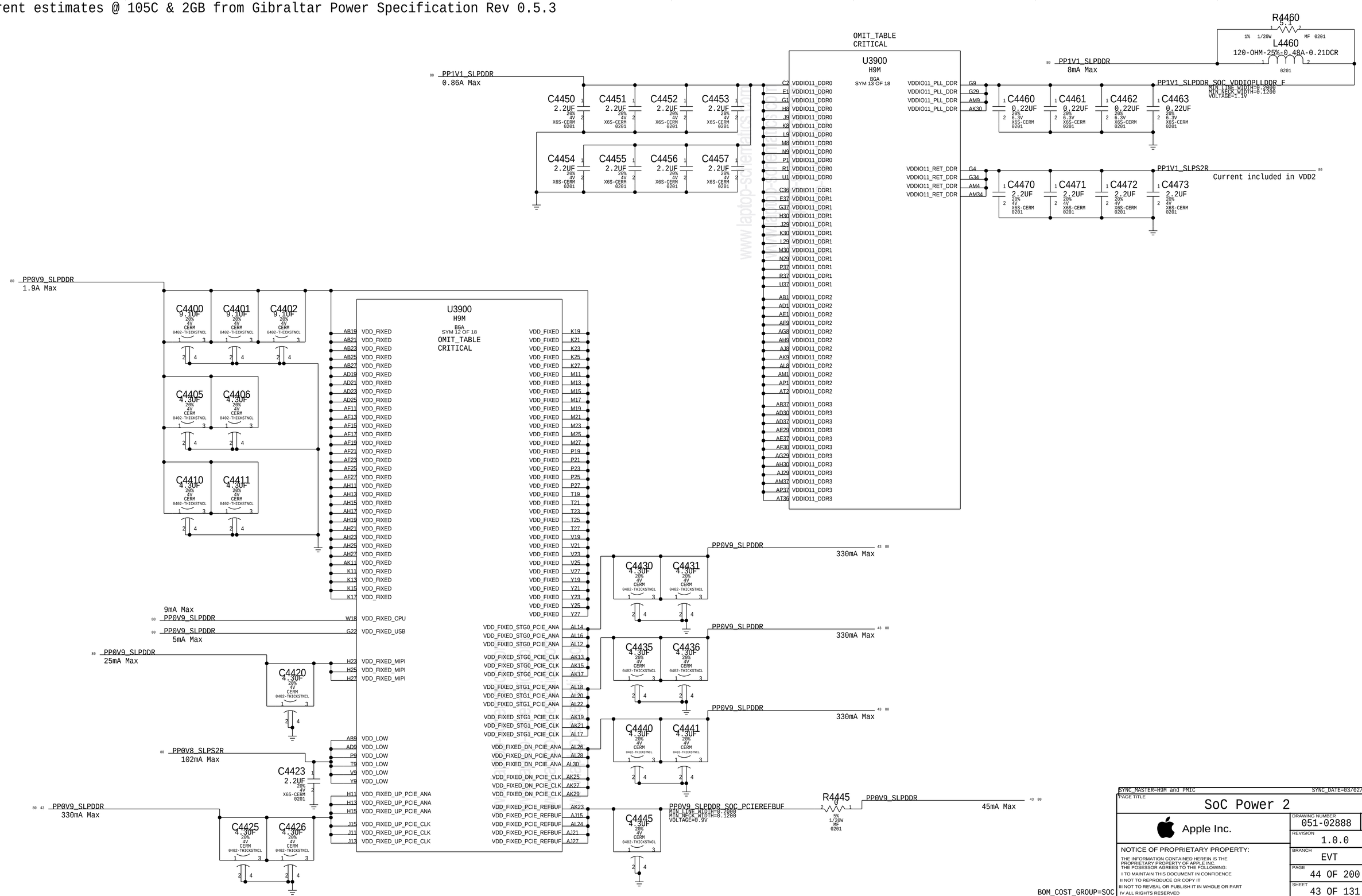
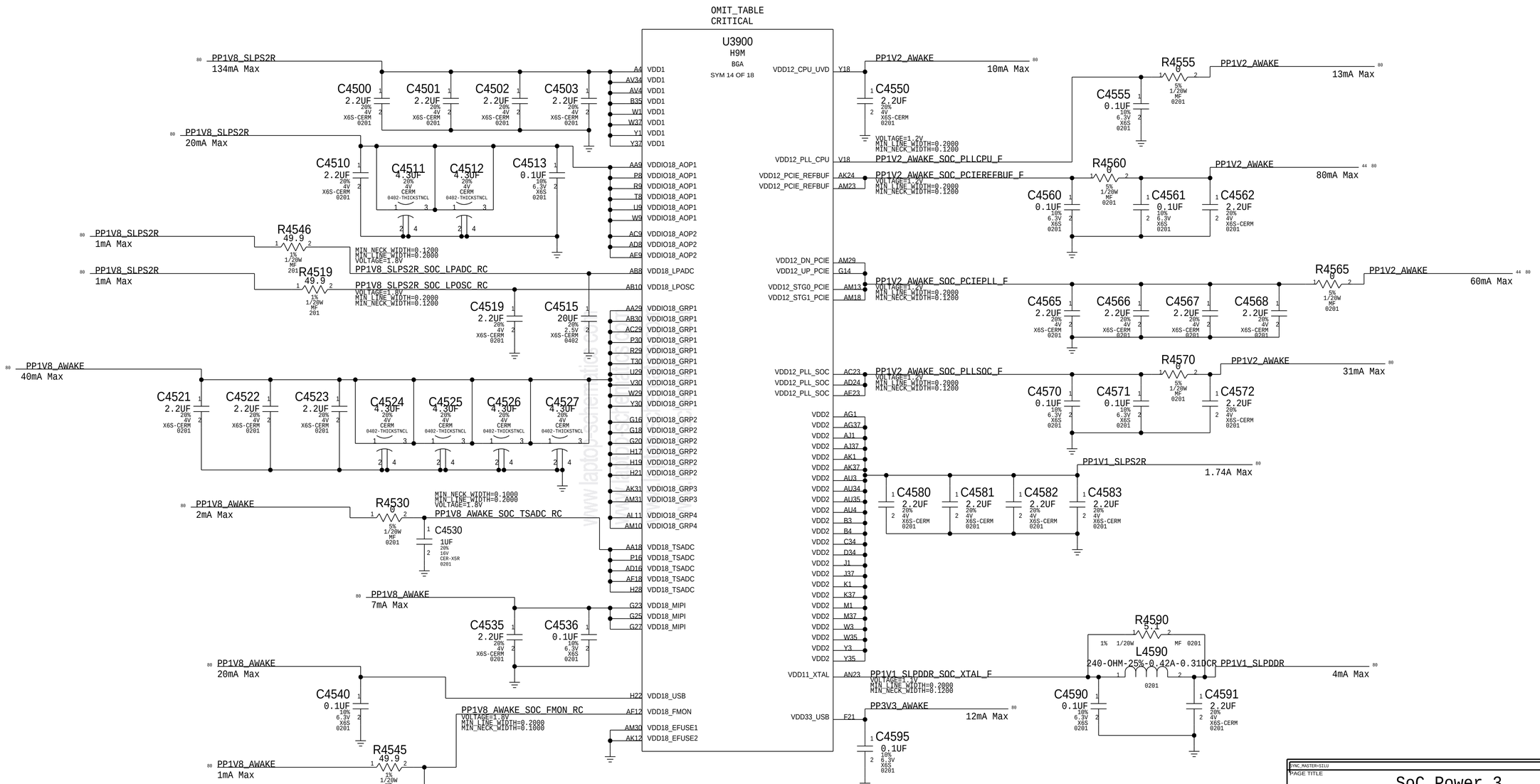
| | PAGE 43 OF 200 |
| | SHEET 42 OF 131 |

BOM_COST_GROUP=SOC

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3




SYNC_MASTER=S1LU SYNC_DATE=05/26/2017

PAGE TITLE

# SoC Power 3

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PAGE 45 OF 200

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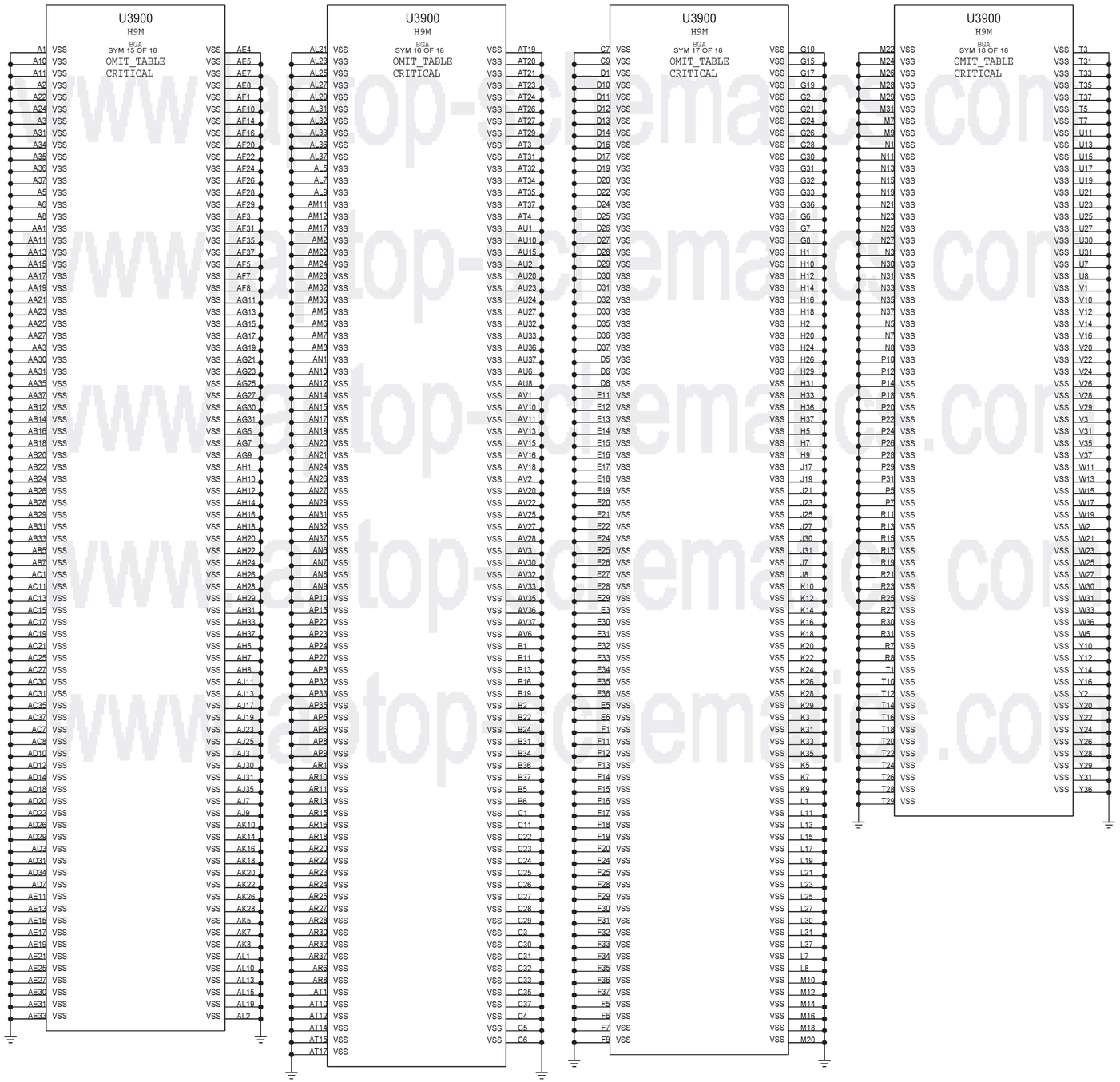


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SYNC_MASTER=H9M and PMIC SYNC_DATE=03/02/2017

PAGE TITLE

# SoC Ground

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PAGE 46 OF 200

SHEET 45 OF 131

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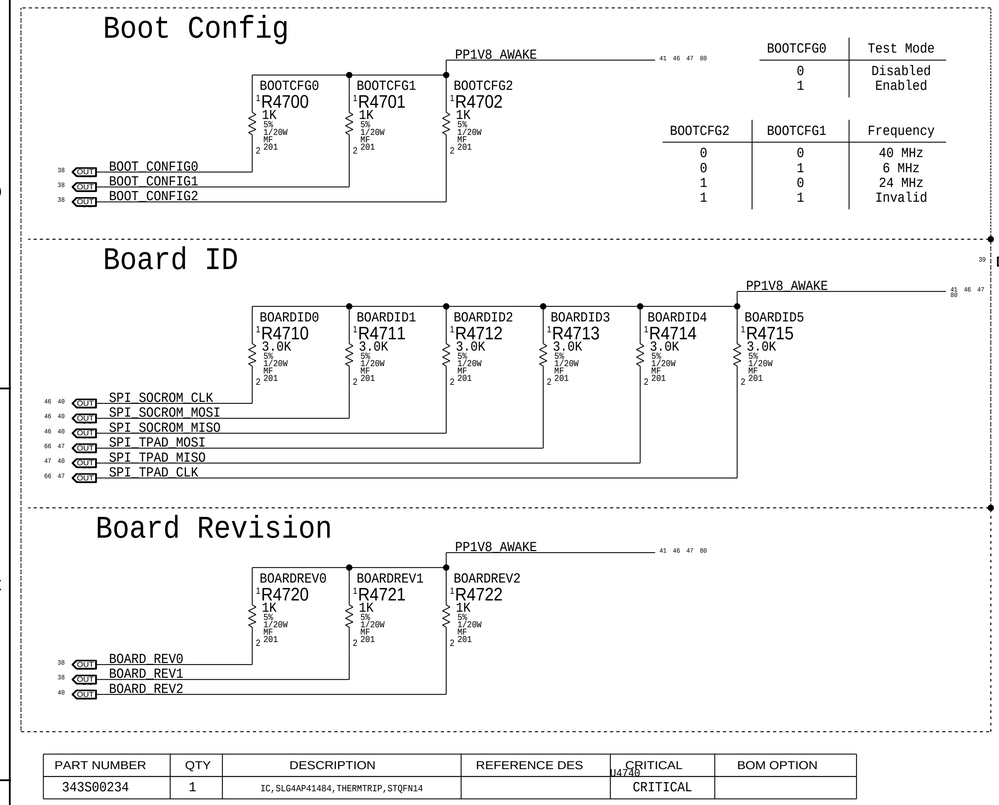
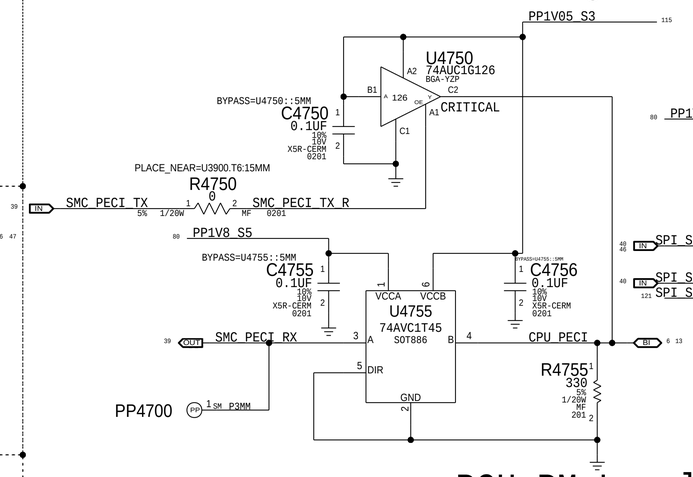



| BOOTCFG0 | Test Mode |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

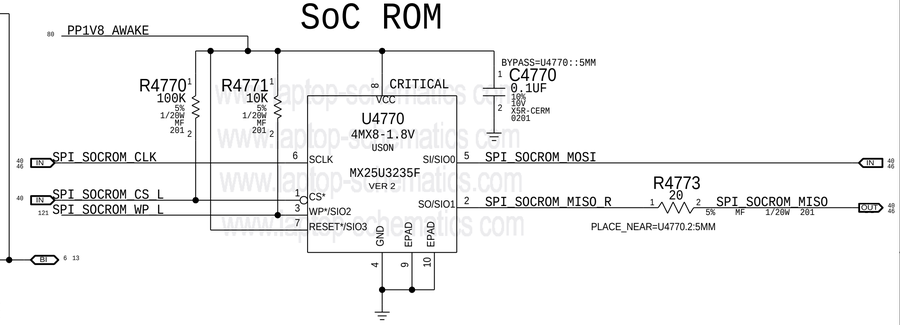
| BOOTCFG2 | BOOTCFG1 | Frequency |
|---|---|---|
| 0 | 0 | 40 MHz |
| 0 | 1 | 6 MHz |
| 1 | 0 | 24 MHz |
| 1 | 1 | Invalid |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 343S00234 | 1 | IC,SLG4AP41484,THERMTRIP,STQFN14 | U4740 | CRITICAL | |

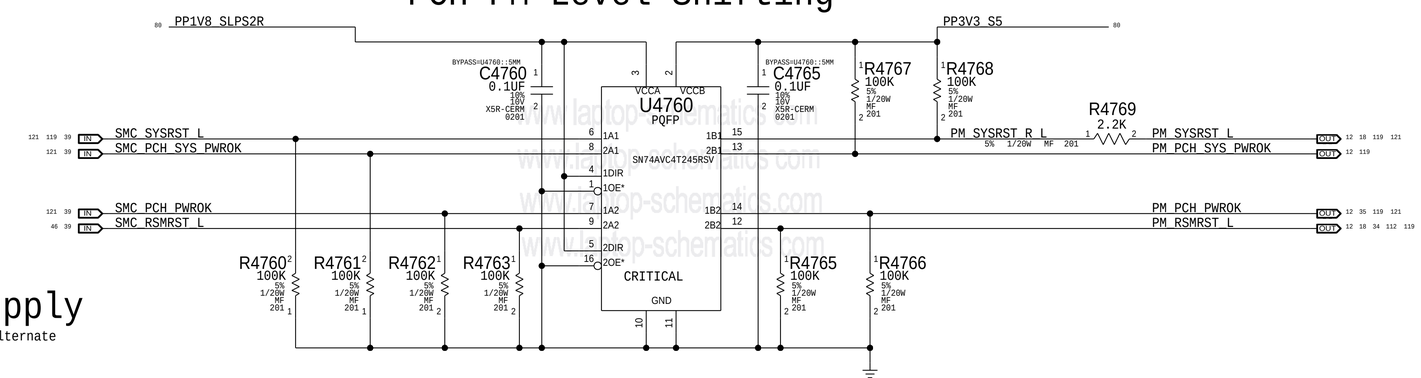
# PECI Level Shifting




# SoC ROM

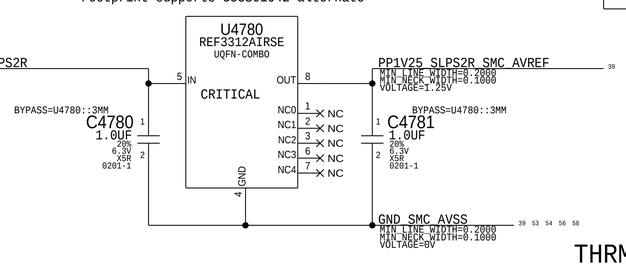



# PCH PM Level Shifting



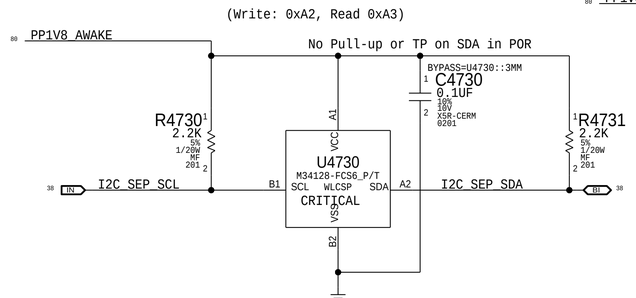

# SMC AVREF Supply

Footprint supports 353S01042 alternate

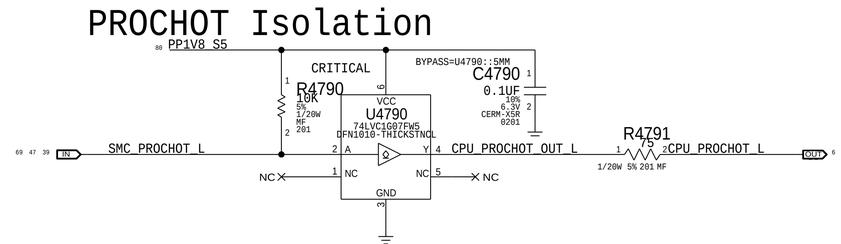



# SEP EEPROM

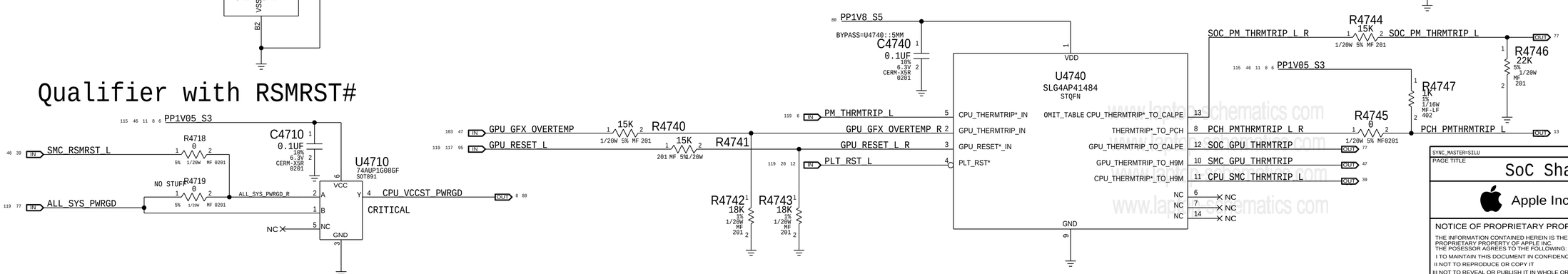
(Write: 0xA2, Read 0xA3)




# PROCHOT Isolation




# THRMTRIP# Isolation




BOM_COST_GROUP=SOC

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SYNC_MASTER=SILU SYNC_DATE=08/09/2017

PAGE TITLE: SoC Shared Support

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0

BRANCH: EVT

PAGE: 47 OF 200

SHEET: 46 OF 131

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## PCIe Up R2D AC Caps

(All Caps)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PCIE_SOC_R2D_C_P<0> | C4820 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_P<0> | | | |
| PCIE_SOC_R2D_C_N<0> | C4821 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_N<0> | | | |
| PCIE_SOC_R2D_C_P<1> | C4822 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_P<1> | | | |
| PCIE_SOC_R2D_C_N<1> | C4823 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_N<1> | | | |
| PCIE_SOC_R2D_C_P<2> | C4824 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_P<2> | | | |
| PCIE_SOC_R2D_C_N<2> | C4825 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_N<2> | | | |
| PCIE_SOC_R2D_C_P<3> | C4826 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_P<3> | | | |
| PCIE_SOC_R2D_C_N<3> | C4827 | 0.22UF | 20% 6.3V X5R 0201 | PCIE_SOC_R2D_N<3> | | | |

## GPIO Source Termination

| | | | | | |
|---|---|---|---|---|---|
| I2S_SPKRAMP_L_R2D_R | R4843 | 20 | PLACE_NEAR=U3900.AG34:5MM | I2S_SPKRAMP_L_R2D | |
| I2S_SPKRAMP_L_BCLK_R | R4844 | 20 | PLACE_NEAR=U3900.AA32:5MM | I2S_SPKRAMP_L_BCLK | |
| I2S_SPKRAMP_L_LRCLK_R | R4863 | 20 | PLACE_NEAR=U3900.AA32:10MM | I2S_SPKRAMP_L_LRCLK | |
| I2S_SPKRAMP_R_R2D_R | R4845 | 20 | PLACE_NEAR=U3900.C20:5MM | I2S_SPKRAMP_R_R2D | |
| I2S_SPKRAMP_R_BCLK_R | R4846 | 20 | PLACE_NEAR=U3900.C21:5MM | I2S_SPKRAMP_R_BCLK | |
| I2S_SPKRAMP_R_LRCLK_R | R4864 | 20 | PLACE_NEAR=U3900.C21:10MM | I2S_SPKRAMP_R_LRCLK | |
| I2S_CODEC_R2D_R | R4847 | 20 | PLACE_NEAR=U3900.AB34:5MM | I2S_CODEC_R2D | |
| I2S_CODEC_BCLK_R | R4848 | 20 | PLACE_NEAR=U3900.AF33:5MM | I2S_CODEC_BCLK | |
| I2S_CODEC_LRCLK_R | R4865 | 20 | PLACE_NEAR=U3900.AF33:5MM | I2S_CODEC_LRCLK | |
| SPI_TPAD_MOSI_R | R4851 | 20 | PLACE_NEAR=U3900.N34:5MM | SPI_TPAD_MOSI | |
| SPI_TPAD_CLK_R | R4852 | 20 | PLACE_NEAR=U3900.P35:5MM | SPI_TPAD_CLK | |
| SPI_MESA_MOSI_R | R4853 | 20 | PLACE_NEAR=U3900.A20:5MM | SPI_MESA_MOSI | |
| SPI_MESA_CLK_R | R4854 | 20 | PLACE_NEAR=U3900.C19:5MM | SPI_MESA_CLK | |
| SPI_DFR_MISO_R | R4866 | 20 | PLACE_NEAR=J5100.7:5MM | SPI_DFR_MISO | |
| SPI_DFR_MOSI_R | R4855 | 20 | PLACE_NEAR=U3900.C18:5MM | SPI_DFR_MOSI | |
| SPI_DFR_CLK_R | R4856 | 20 | PLACE_NEAR=U3900.B18:5MM | SPI_DFR_CLK | |
| SSD0_CLK24M_R | R4857 | 20 | PLACE_NEAR=U3900.AP7:5MM | SSD0_CLK24M | |
| SSD1_CLK24M_R | R4858 | 20 | PLACE_NEAR=U3900.AV7:5MM | SSD1_CLK24M | S4E_X4PLUS |
| PDM_DMIC_CLK0_R | R4859 | 20 | PLACE_NEAR=U3900.P6:15MM | PDM_DMIC_CLK0 | |
| PDM_DMIC_CLK1_R | R4860 | 20 | PLACE_NEAR=U3900.K2:15MM | PDM_DMIC_CLK1 | |
| SPI_AOP_SENSOR_MOSI_R | R4861 | 20 | PLACE_NEAR=U3900.D2:10MM | SPI_AOP_SENSOR_MOSI | |
| SPI_AOP_SENSOR_CLK_R | R4862 | 20 | PLACE_NEAR=U3900.F2:15MM | SPI_AOP_SENSOR_CLK | |
| SPI_AOP_SENSOR_MISO_R | R4869 | 20 | PLACE_NEAR=U3900.E2:15MM | SPI_AOP_SENSOR_MISO | |
| SPI_TPAD_MISO | R4809 | 20 | PLACE_NEAR=U3900.P36:20MM | SPI_TPAD_MISO_R | |

## Lifeboat

| | | |
|---|---|---|
| PCIE_LIFEBOAT_R2D_C_P | PCIE_LIFEBOAT_R2D_C_P | TP4800 |
| PCIE_LIFEBOAT_R2D_C_N | PCIE_LIFEBOAT_R2D_C_N | TP4801 |
| PCIE_LIFEBOAT_D2R_P | PCIE_LIFEBOAT_D2R_P | TP4802 |
| PCIE_LIFEBOAT_D2R_N | PCIE_LIFEBOAT_D2R_N | TP4803 |
| PCIE_CLK100M_LIFEBOAT_P | PCIE_CLK100M_LIFEBOAT_P | TP4804 |
| PCIE_CLK100M_LIFEBOAT_N | PCIE_CLK100M_LIFEBOAT_N | TP4805 |
| PCIE_LIFEBOAT_CLKREQ_L | PCIE_LIFEBOAT_CLKREQ_L | TP4806 |
| PCIE_LIFEBOAT_RESET_L | PCIE_LIFEBOAT_RESET_L | TP4807 |

SMC_FIXTURE_MODE_L — SMC_FIXTURE_MODE_L

FIXMODE_NO — R4801 100K 5% 1/20W MF 201

## Lid Detect Sensors

Clamshell Open = High
Clamshell Closed = Low

OMIT_TABLE J4800 AMR-MLB-X502 — PP1V8_SLPS2R — R4807 330K 5% 1/20W MF 201 — AMR_PU — SMC_LID_LEFT — R4804 10K 5% 1/20W MF 201 — LID_OPEN_LEFT

OMIT_TABLE J4801 AMR-MLB-X502 — PP1V8_SLPS2R — R4808 330K 5% 1/20W MF 201 — AMR_PU — SMC_LID_RIGHT — R4805 10K 5% 1/20W MF 201 — LID_OPEN_RIGHT

PP1V8_SLPS2R — C4802 0.1UF 10% 6.3V CERM-X5R 0201 — U4802 74LVC1G32 SOT891 — IPD_LID_OPEN

## No Connects

| | | |
|---|---|---|
| NC_SPI_ALTIMETER_CS_L | NC_SPI_ALTIMETER_CS_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_ALTIMETER_INT | NC_ALTIMETER_INT | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PMU_CLK32K_GNSS_R | NC_PMU_CLK32K_GNSS_R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_UART_GNSS_D2R_CTS_L | NC_UART_GNSS_D2R_CTS_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_UART_GNSS_R2D_RTS_L | NC_UART_GNSS_R2D_RTS_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_GNSS_HOST_TIME | NC_GNSS_HOST_TIME | MAKE_BASE=TRUE NO_TEST=1 |
| NC_GNSS_HOST_WAKE | NC_GNSS_HOST_WAKE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_GNSS_DEV_WAKE | NC_GNSS_DEV_WAKE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_ENET_MEDIA_SENSE | NC_ENET_MEDIA_SENSE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_ENET_LOW_PWR | NC_ENET_LOW_PWR | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_HAWKING_D2R | NC_I2S_HAWKING_D2R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_HAWKING_LRCLK | NC_I2S_HAWKING_LRCLK | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_HAWKING_BCLK | NC_I2S_HAWKING_BCLK | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_CODEC1_R2D_R | NC_I2S_CODEC1_R2D_R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_RX_CLK12M_R | NC_PLCAM_RX_CLK12M_R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_RX_RESET_L | NC_PLCAM_RX_RESET_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_TX_CLK12M_R | NC_PLCAM_TX_CLK12M_R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_TX_RESET_L | NC_PLCAM_TX_RESET_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_TX_INT | NC_PLCAM_TX_INT | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_TX_THROTTLE | NC_PLCAM_TX_THROTTLE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_PROX_INT_L | NC_PLCAM_PROX_INT_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PLCAM_ROMEO_B2B_DETECT | NC_PLCAM_ROMEO_B2B_DETECT | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCHROM_SW_EN | NC_PCHROM_SW_EN | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SDCONN_STATE_CHANGE_L | NC_SDCONN_STATE_CHANGE_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_FTCAM_RESET_L | NC_FTCAM_RESET_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_FTCAM_CLK12M_R | NC_FTCAM_CLK12M_R | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_CODEC_MCLK | NC_I2S_CODEC_MCLK | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2S_CODEC1_MCLK | NC_I2S_CODEC1_MCLK | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SPI_DSCRPTR_OVERRIDE_L | NC_SPI_DSCRPTR_OVERRIDE_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2C_AOP_SCL | NC_I2C_AOP_SCL | MAKE_BASE=TRUE NO_TEST=1 |
| NC_I2C_AOP_SDA | NC_I2C_AOP_SDA | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SOC_USB_ID | NC_SOC_USB_ID | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SOC_TST_CLKOUT | NC_SOC_TST_CLKOUT | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SOC_AMUXOUT | NC_SOC_AMUXOUT | MAKE_BASE=TRUE NO_TEST=1 |

| | | |
|---|---|---|
| NC_SPKR_ID1 | NC_SPKR_ID1 | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SMC_LED_ONEWIRE | NC_SMC_LED_ONEWIRE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIEDN_WAKE_L | NC_PCIEDN_WAKE_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_MESA_MENUKEY_L | NC_MESA_MENUKEY_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_TPAD_VIBE_L | NC_TPAD_VIBE_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_ENET_RESET_L | NC_ENET_RESET_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_WLAN_DEV_WAKE | NC_WLAN_DEV_WAKE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SOC_VSSCPU_SENSE | NC_SOC_VSSCPU_SENSE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_SOC_VSSSOC_SENSE | NC_SOC_VSSSOC_SENSE | MAKE_BASE=TRUE NO_TEST=1 |
| NC_DFR_TOUCH_RSVD | NC_DFR_TOUCH_RSVD | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_DN3_R2D_CP | NC_PCIE_DN3_R2D_CP | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_DN3_R2D_CN | NC_PCIE_DN3_R2D_CN | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_DN3_D2RP | NC_PCIE_DN3_D2RP | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_DN3_D2RN | NC_PCIE_DN3_D2RN | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_CLK100M_DN3P | NC_PCIE_CLK100M_DN3P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_CLK100M_DN3N | NC_PCIE_CLK100M_DN3N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIEDN3_CLKREQ_L | NC_PCIEDN3_CLKREQ_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIEDN3_RESET_L | NC_PCIEDN3_RESET_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_WLAN_R2D_C_P | NC_PCIE_WLAN_R2D_C_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_WLAN_R2D_C_N | NC_PCIE_WLAN_R2D_C_N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_WLAN_D2R_P | NC_PCIE_WLAN_D2R_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_WLAN_D2R_N | NC_PCIE_WLAN_D2R_N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_WLAN_CLKREQ_L | NC_WLAN_CLKREQ_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_WLAN_PERST_L | NC_WLAN_PERST_L | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_ENET_R2D_C_P | NC_PCIE_ENET_R2D_C_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_ENET_R2D_C_N | NC_PCIE_ENET_R2D_C_N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_ENET_D2R_P | NC_PCIE_ENET_D2R_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_ENET_D2R_N | NC_PCIE_ENET_D2R_N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_CLK100M_ENET_P | NC_PCIE_CLK100M_ENET_P | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_CLK100M_ENET_N | NC_PCIE_CLK100M_ENET_N | MAKE_BASE=TRUE NO_TEST=1 |
| NC_PCIE_CLK100M_WLAN_P | NC_PCIE_CLK100M_WLAN_P | MAKE_BASE NO_TEST=1 |
| NC_PCIE_CLK100M_WLAN_N | NC_PCIE_CLK100M_WLAN_N | MAKE_BASE NO_TEST=1 |

## Signal Aliases

| | | |
|---|---|---|
| TPAD_KBD_WAKE_L | TPAD_KBD_WAKE_L | MAKE_BASE |
| TPAD_SPI_INT_L | TPAD_SPI_INT_L | MAKE_BASE |
| TPAD_ACTUATOR_DISABLE_L | TPAD_ACTUATOR_DISABLE_L | MAKE_BASE |
| GPU_GFX_OVERTEMP | GPU_GFX_OVERTEMP | MAKE_BASE |
| SMC_DEBUGPRT_RX | SMC_DEBUGPRT_RX | MAKE_BASE |
| SMC_DEBUGPRT_TX | SMC_DEBUGPRT_TX | MAKE_BASE |
| SMC_GPU_THRMTRIP | SMC_GPU_THRMTRIP | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |
| GND | GND | MAKE_BASE |

| | | |
|---|---|---|
| SOC_VDDSOC_SENSE | P3MM SM | PP4800 |
| SOC_VDDCPU_SENSE | P3MM SM | PP4801 |
| SSD0_OCARINA_WP_L | P5MM-SP SM-SP | PP4802 |
| SSD1_OCARINA_WP_L | P5MM-SP SM-SP | PP4803 |
| SMC_PROCHOT_L | P3MM SM | PP4808 |

| | | |
|---|---|---|
| SWD_SOC_SWCLK | MAKE_BASE=TRUE | SWD_SOC_SWCLK |
| SWD_SOC_SWDIO | MAKE_BASE=TRUE | SWD_SOC_SWDIO |

INT PU SOC 50k

CHGR_INT_L — PLACE_SIDE=BOTTOM — SM P2MM — PP4809

| | | | |
|---|---|---|---|
| MIPI_FTCAM_DATA_P<0> | PLACE_NEAR=U3900.B27:10MM | SM P2MM | PP4804 |
| MIPI_FTCAM_DATA_N<0> | PLACE_NEAR=U3900.A26:10MM | SM P2MM | PP4805 |
| MIPI_FTCAM_CLK_P | PLACE_NEAR=U3900.B26:10MM | SM P2MM | PP4806 |
| MIPI_FTCAM_CLK_N | PLACE_NEAR=U3900.A26:10MM | SM P2MM | PP4807 |

PP1V8_SLPS2R
PP1V8_AWAKE

| | | | | |
|---|---|---|---|---|
| R4883 | 47K | | | SSD0_CLKREQ0_L |
| R4884 | 47K | | | SSD0_CLKREQ1_L |
| R4887 | 47K | | | SSD0_CLKREQ2_L |
| R4888 | 47K | | | SSD0_CLKREQ3_L |
| R4889 | 47K | S4E_X4PLUS | | SSD1_CLKREQ0_L |
| R4890 | 47K | S4E_X4PLUS | | SSD1_CLKREQ1_L |
| R4891 | 47K | S4E_X4PLUS | | SSD1_CLKREQ2_L |
| R4892 | 47K | S4E_X4PLUS | | SSD1_CLKREQ3_L |
| R4895 | 100K | | | SSD_PMU_RESET_L |
| R4885 | 100K | | | SSD0_PCIE_RESET_L |
| R4886 | 47K | S4E_X4PLUS | | SSD0_CLK24M |
| R4893 | 100K | S4E_X4PLUS | | SSD1_PCIE_RESET_L |
| R4894 | 47K | | | SSD1_CLK24M |
| R4870 | 0 | | | I2S_SPKRAMP_R_D2R |

| | BOM GROUP | BOM OPTIONS |
|---|---|---|
| Proto 0 | BOARD_REV:111 | BOARDREV2,BOARDREV1,BOARDREV0 |
| Proto 1 | BOARD_REV:110 | BOARDREV2,BOARDREV1 |
| Proto 2 | BOARD_REV:101 | BOARDREV2,BOARDREV0 |
| Pre-EVT | BOARD_REV:100 | BOARDREV2 |
| EVT | BOARD_REV:011 | BOARDREV1,BOARDREV0 |
| DVT | BOARD_REV:010 | BOARDREV1 |
| PVT | BOARD_REV:001 | BOARDREV0 |
| | BOARD_REV:000 | |

BOM_COST_GROUP=SOC

PAGE TITLE
# SoC Project Support

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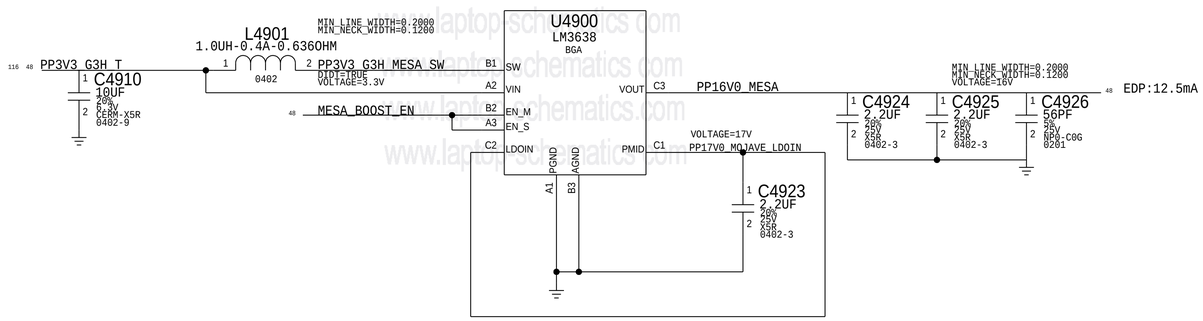
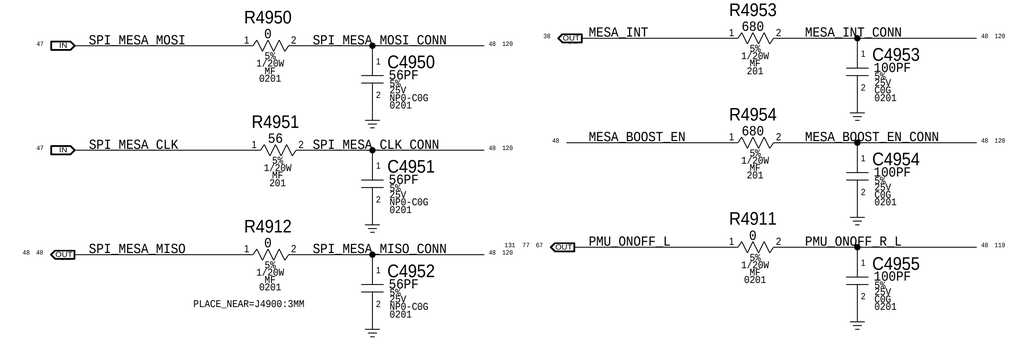
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
| BRANCH | EVT |
| PAGE | 48 OF 200 |
| SHEET | 47 OF 131 |

ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

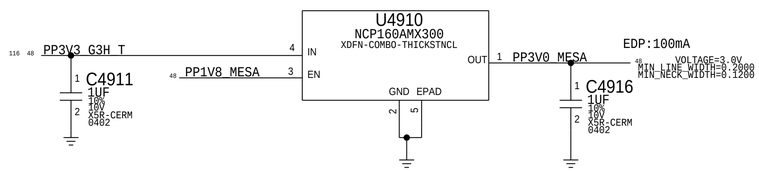
## MOJAVE 16V BOOST

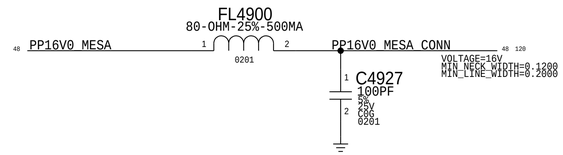


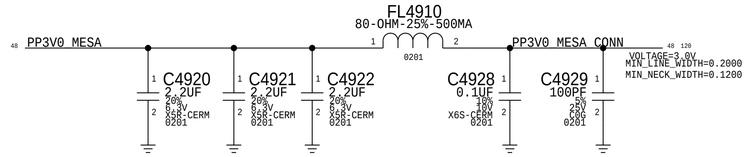




## 3.0V MESA

Option to feed LDO from 5V in case of dropout issue

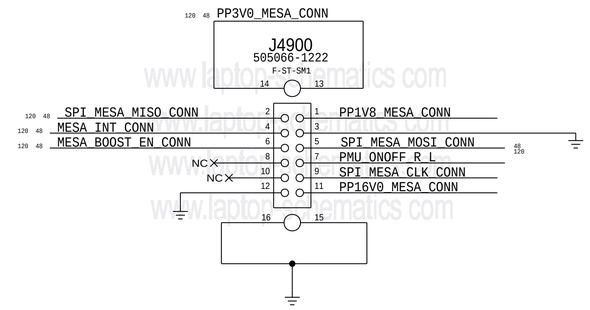



## MESA FLEX CONNECTOR

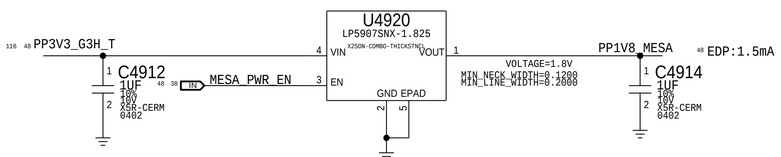
Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

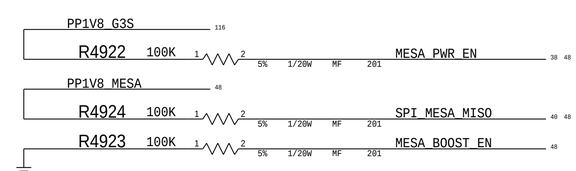



Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

## 1.8V MESA



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|---|---|
| PAGE TITLE | MESA |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
| | REVISION 1.0.0 |
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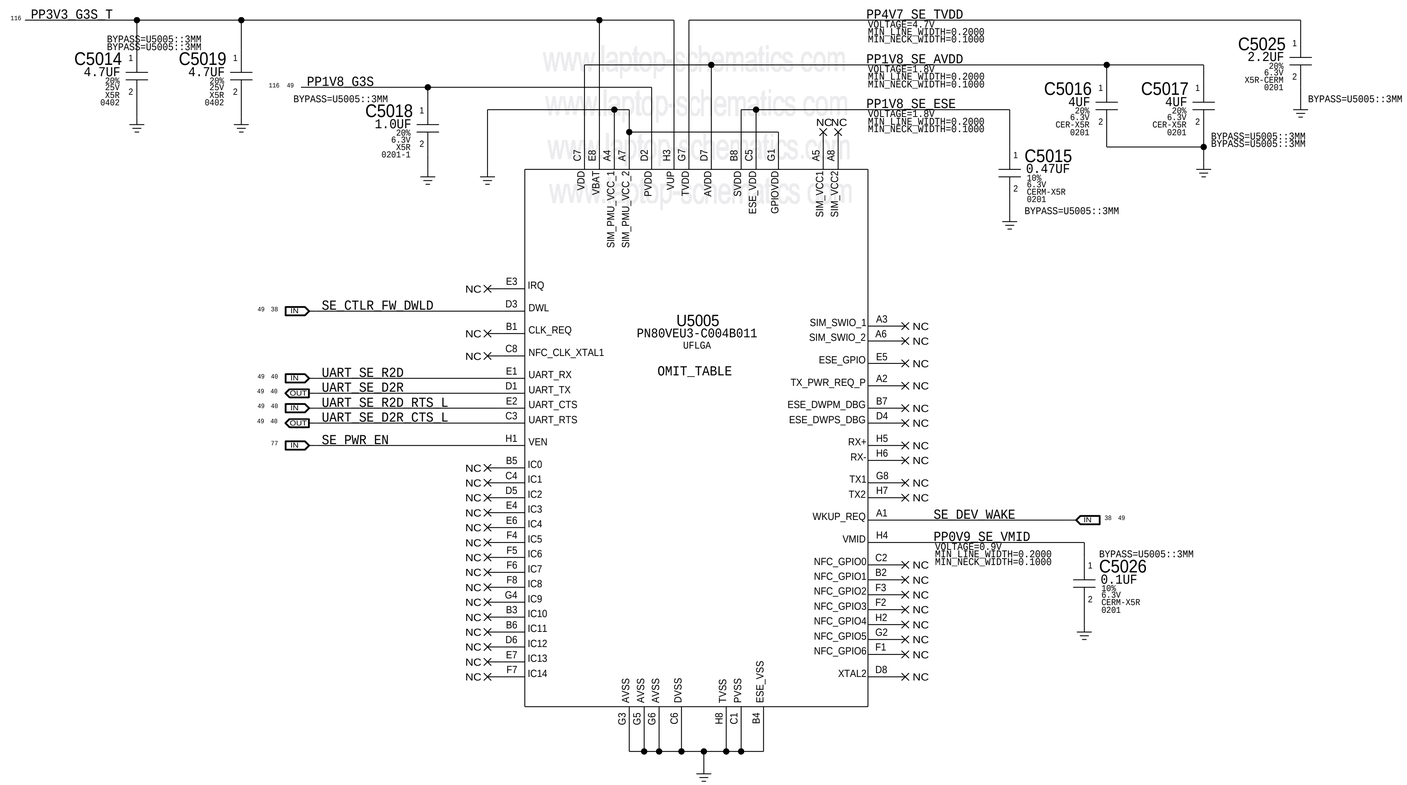
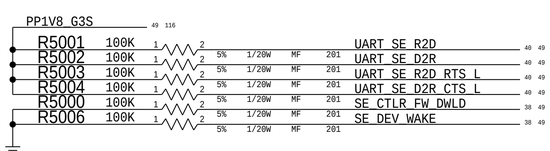



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 998-11132 | 1 | IC,RTM4,ES2.1,PN80V,DEV,UFLGA64 | U5005 | CRITICAL | SE:DEV_2017 |
| 338S00253 | 1 | IC,RTM4,ES2.1,PN80V,PRD,UFLGA64 | U5005 | CRITICAL | SE:PROD_2017 |

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SYNC_MASTER=S1LU SYNC_DATE=05/05/2017

PAGE TITLE: Secure Element

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DRAWING NUMBER: 051-02888 SIZE: D

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SHEET: 49 OF 131

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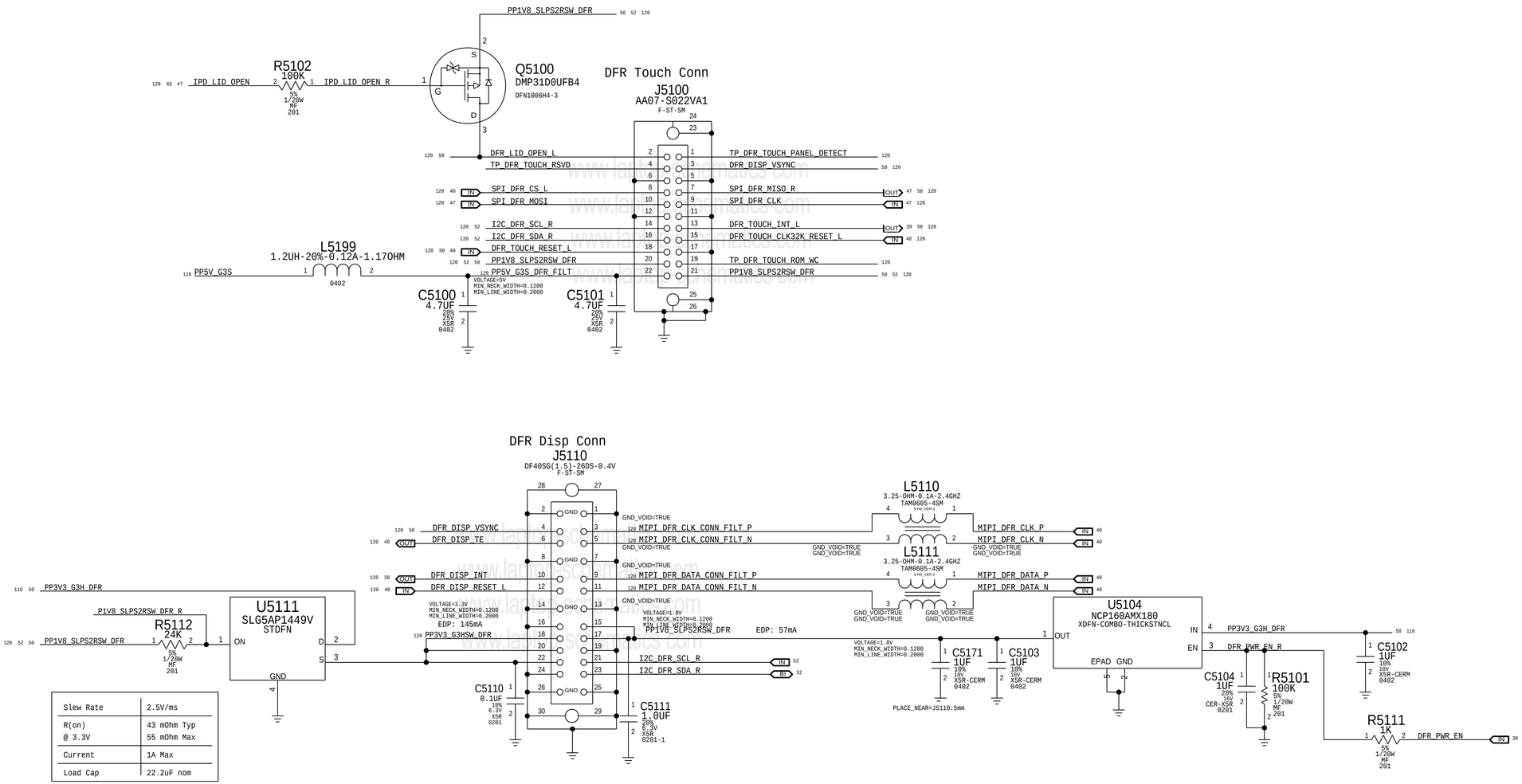
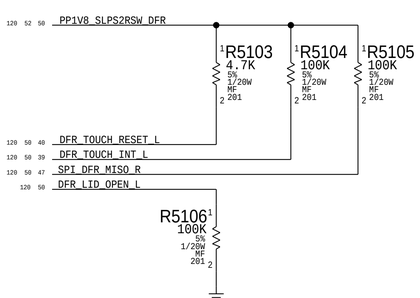
# T208 Support




| Slew Rate | 2.5V/ms |
|---|---|
| R(on) @ 3.3V | 43 mOhm Typ<br>55 mOhm Max |
| Current | 1A Max |
| Load Cap | 22.2uF nom |

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PAGE TITLE: DFR & T208 Support

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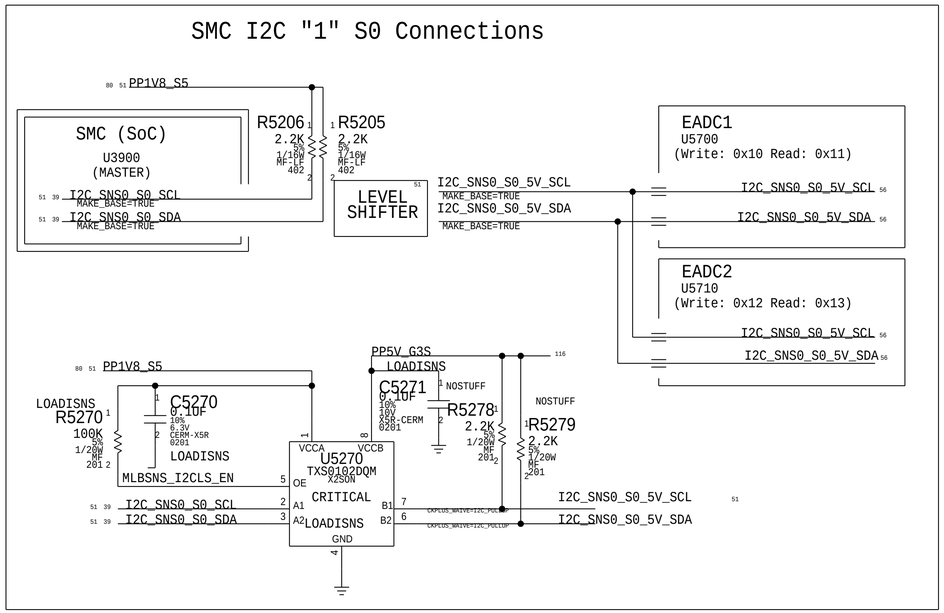
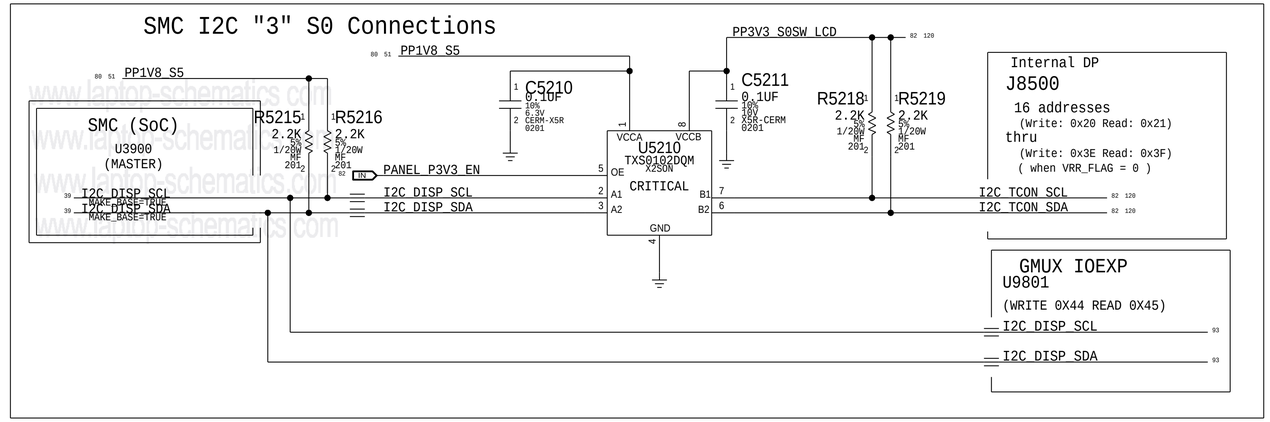
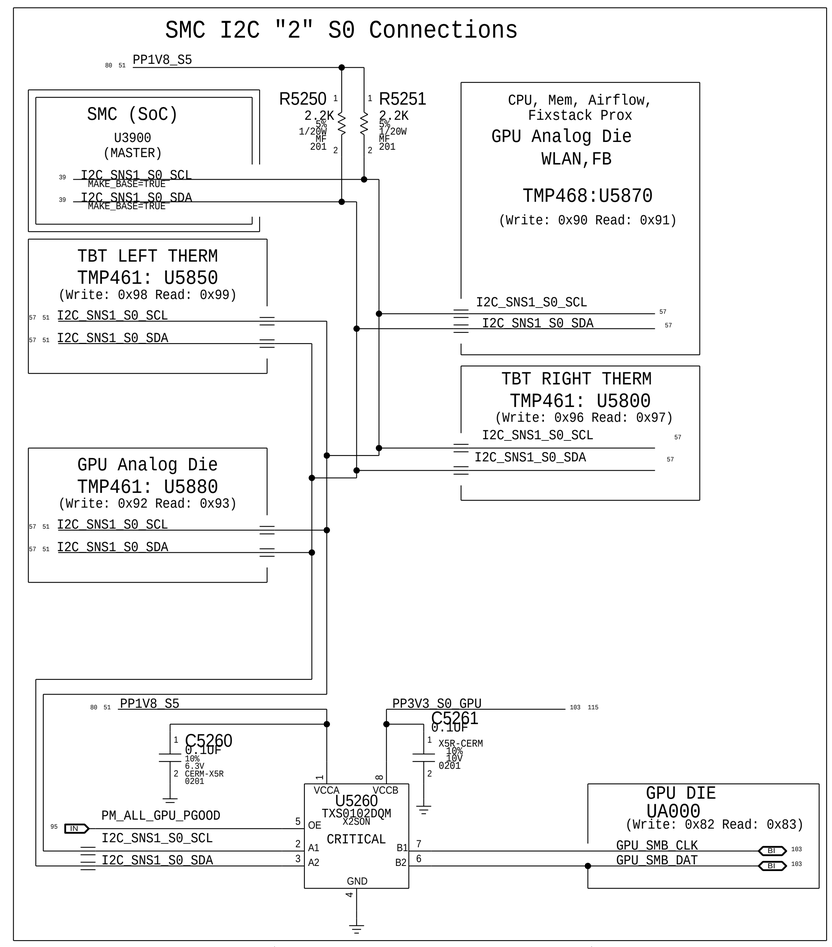
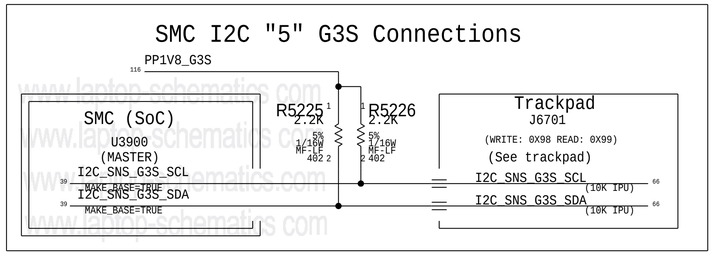
PAGE: 51 OF 200
SHEET: 50 OF 131

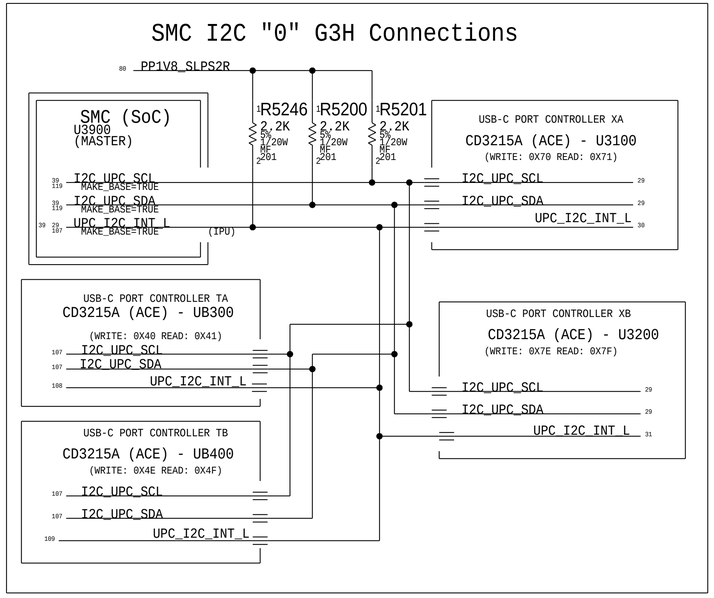


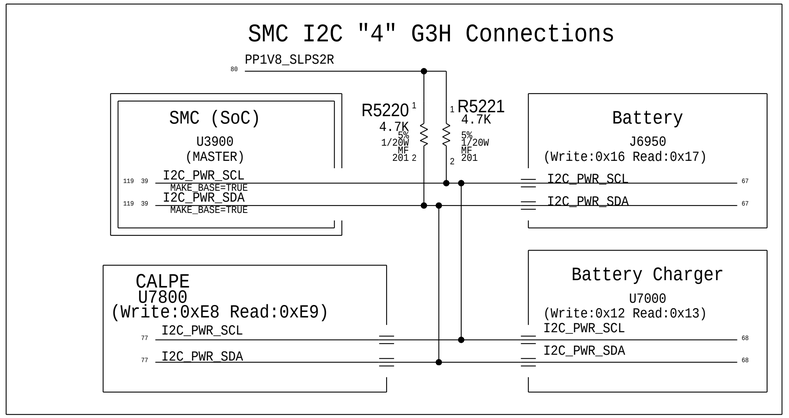



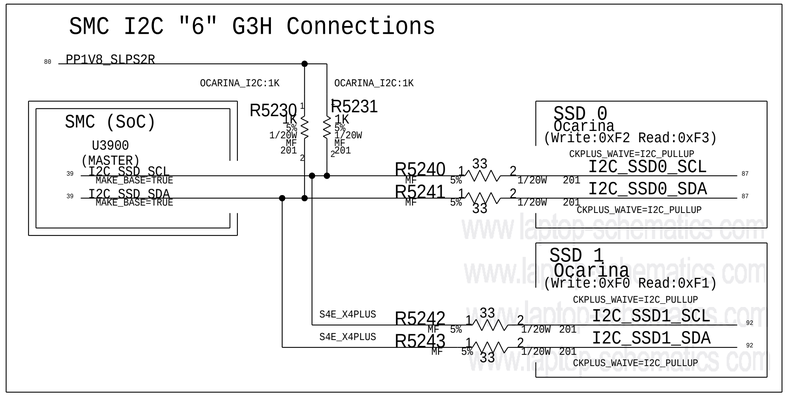

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0059 | 2 | RES,2.2K,1/20W,0201,SMD,MF | R5230,R5231 | | OCARINA_I2C:2.2K |




BOM_COST_GROUP=SMC

PAGE TITLE

# I2C Connections 1

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 52 OF 200

SHEET 51 OF 131

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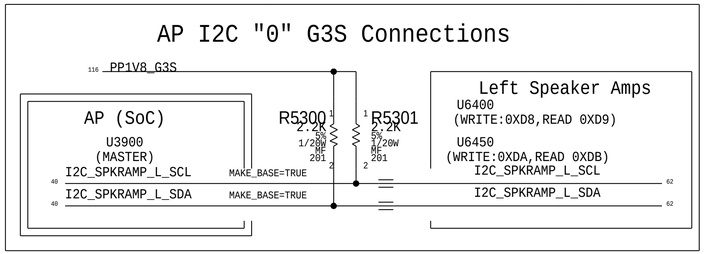


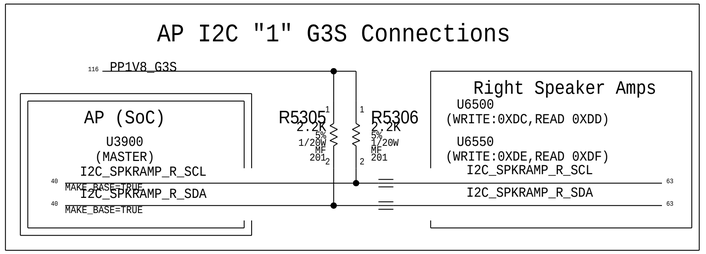


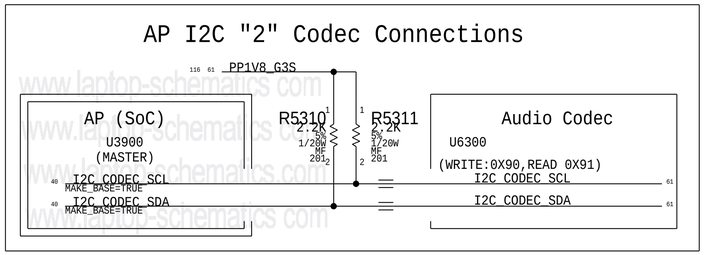


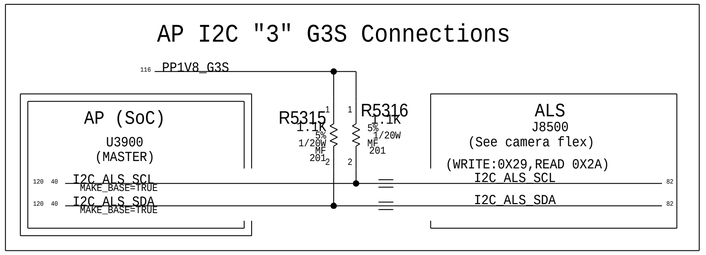


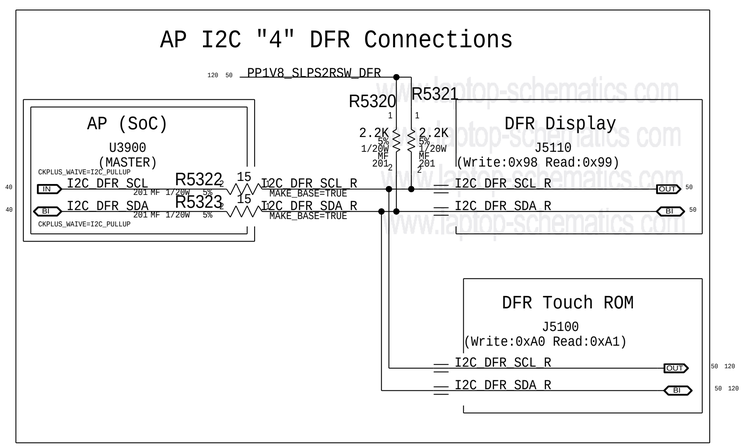


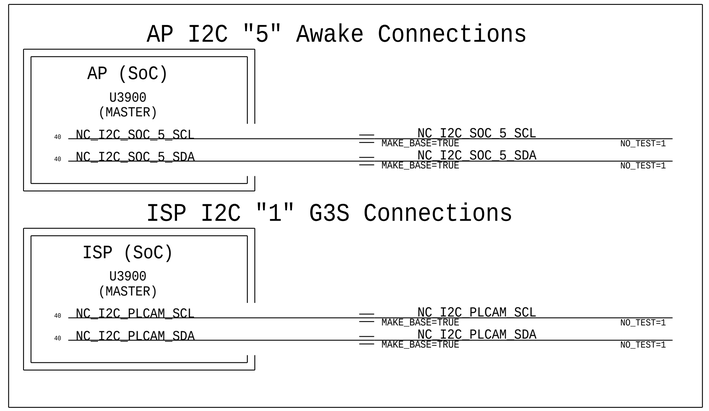


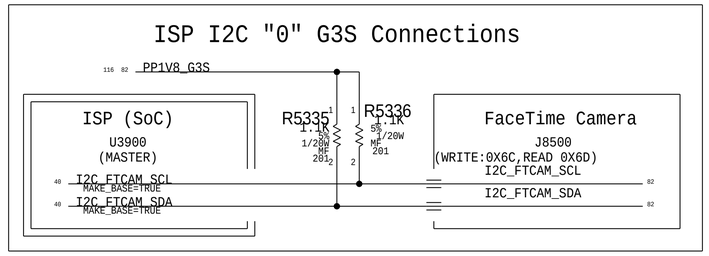


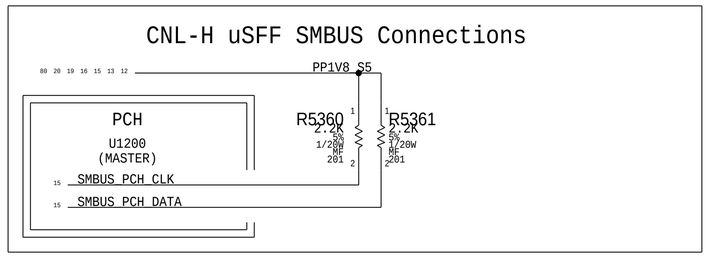


## I2C Device Address

| Device | SMC IF | ADDR. (8b) |
|---|---|---|
| ACE XA | I2C0 | 0X70/1 |
| ACE XB | I2C0 | 0X7E/F |
| ACE TA | I2C0 | 0X40/1 |
| ACE TB | I2C0 | 0X4E/F |
| EADC1 | I2C1 | 0X10/1 |
| EADC2 | I2C1 | 0X12/3 |
| Temp. Sensor Left | I2C2 | 0X98/9 |
| Temp. Sensor Right | I2C2 | 0X96/7 |
| CPU,MEM,WLAN Thermal | I2C2 | 0X90/1 |
| GPU Analog Die Thermal | I2C2 | 0X92/3 |
| GPU Digital Die Thermal | I2C2 | 0X82/3 |
| TCON | I2C3 | 0X20-3F |
| GMUX IOEXP | I2C3 | 0X44/5 |
| Charger | I2C4 | 0X12/3 |
| Battery | I2C4 | 0X16/7 |
| Calpe | I2C4 | 0XE8/9 |
| Trackpad | I2C5 | 0X98/9 |
| SSD0 | I2C6 | 0XF2/3 |
| SSD1 | I2C6 | 0XF0/1 |
| SoC IF | | |
| Left Spkr Amp.(U6400) | I2C0 | 0XD8/9 |
| Left Spkr Amp.(U6450) | I2C0 | 0XDA/B |
| Right Spkr Amp.(U6500) | I2C1 | 0XDC/D |
| Right Spkr Amp.(U6550) | I2C1 | 0XDE/F |
| Audio Codec | I2C2 | 0X90/1 |
| ALS | I2C3 | 0X29/A |
| DFR Display | I2C4 | 0X98/9 |
| DFR Touch | I2C4 | 0XA0/1 |
| NC. | I2C5 | |
| NC. Spkr ID1 | I2C6_SDA | |
| Spkr ID0 | I2C6_SCL | |
| ISP IF | | |
| FT Camera | I2C0 | 0X6C/D |
| NC. | I2C1 | |
| AOP IF | | |
| NC. | I2C0 | |
| PCH IF | | |
| NC. | PULL-UP | |

BOM_COST_GROUP=SMC

PAGE TITLE
I2C Connections 2

Apple Inc.

DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 53 OF 200
SHEET 52 OF 131

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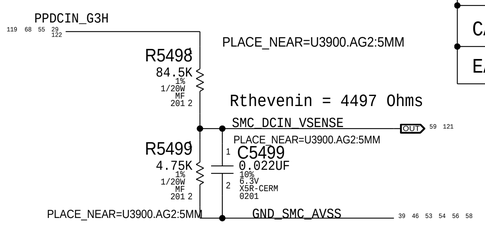
## DC-IN Voltage Sense (VD0R)

Gain: 0.05322x
Vnominal: 20 V, Range: 23.49 V
SMC ADC: 00
Enables DC-In VSense divider when AC present.
2.2KHz

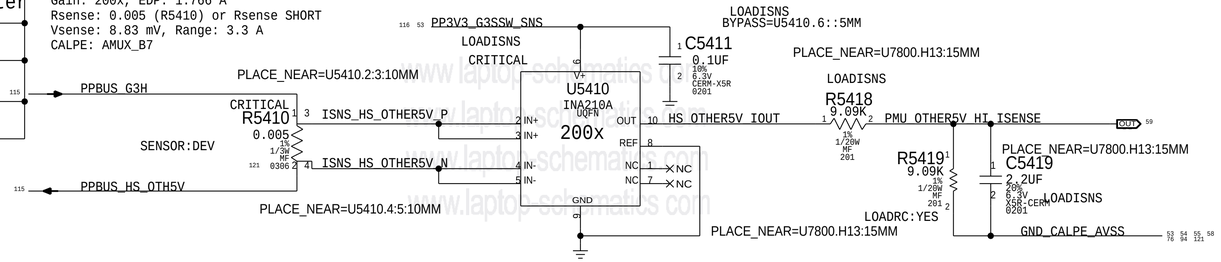



J680 SENSOR SETTINGS

| CHIP | Vref(V) | Vmax | SMC sample Freq. | ADR RC filter |
|---|---|---|---|---|
| H9M | 1.25 | 1.8 | 10khz | 0.1ms |
| CALPE | 1.5 | 5 | 100hz | 10ms |
| EADC | 2.5 | 5 | 1-2hz(10hz) | 100ms |

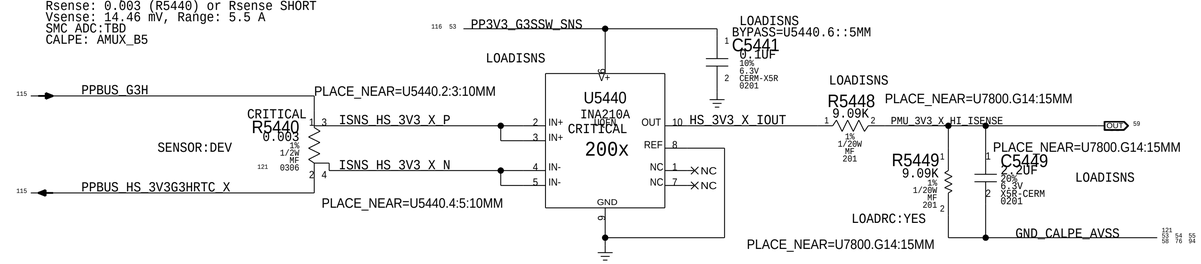
## OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.766 A
Rsense: 0.005 (R5410) or Rsense SHORT
Vsense: 8.83 mV, Range: 3.3 A
CALPE: AMUX_B7



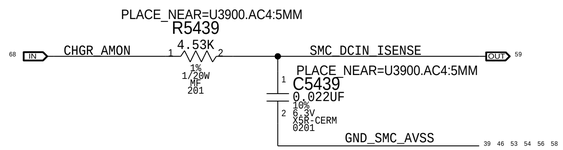

## LEFT SIDE 3.3V High Side Current Sense (IOLR)

Gain: 200x, EDP: 4.82 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 14.46 mV, Range: 5.5 A
SMC ADC:TBD
CALPE: AMUX_B5



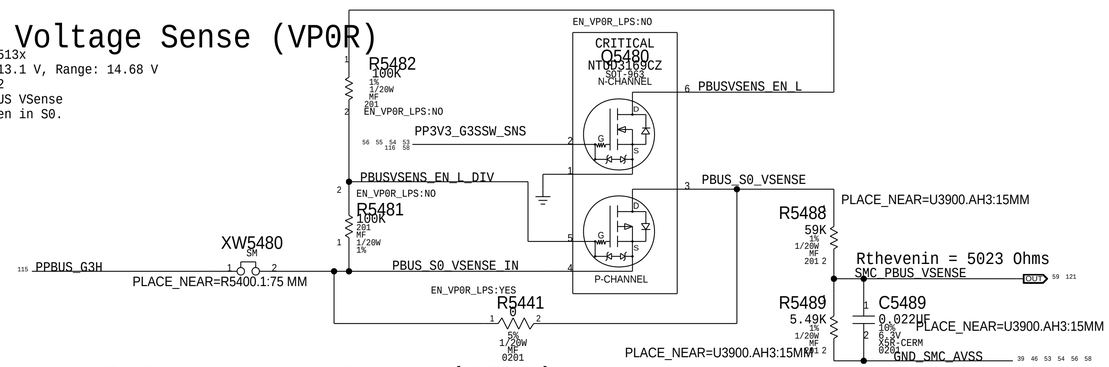

## DC-IN Current Sense (ID0R)

DISCharger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 01



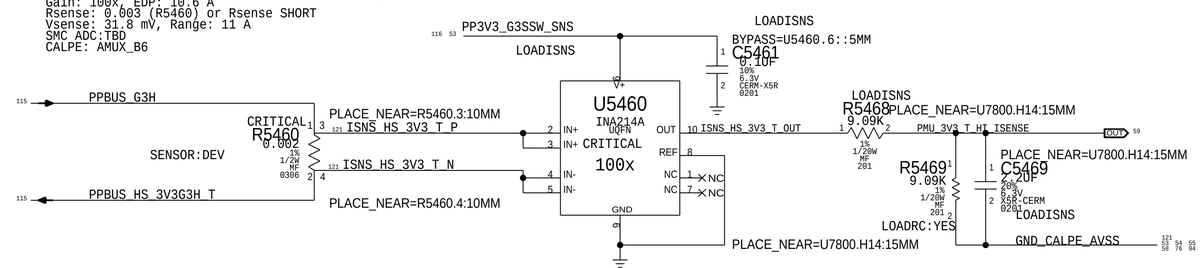

## PBUS Voltage Sense (VP0R)

Gain: 0.08513x
Vnominal: 13.1 V, Range: 14.68 V
SMC ADC: 02
Enables PBUS VSense divider when in S0.



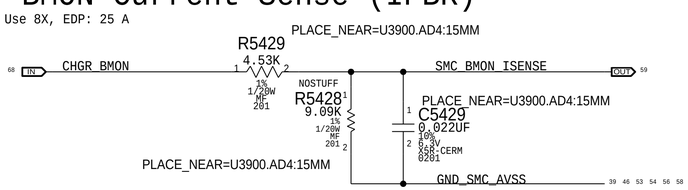

## RIGHT SIDE 3.3V High Side Current Sense (IORR)

Gain: 100x, EDP: 10.6 A
Rsense: 0.003 (R5460) or Rsense SHORT
Vsense: 31.8 mV, Range: 11 A
SMC ADC:TBD
CALPE: AMUX_B6



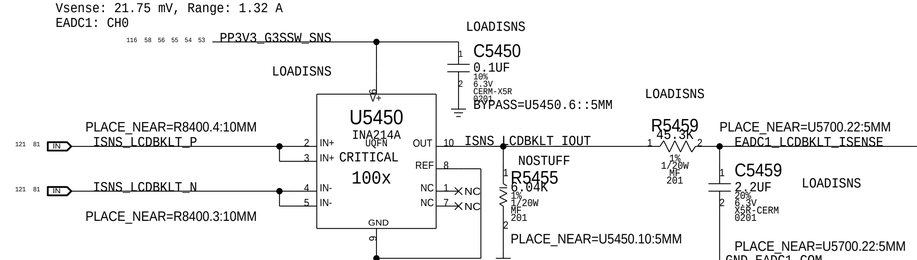

## Discharger BMON Current Sense (IPBR)

Charger Gain: 8X OR 64x, Use 8X, EDP: 25 A
Rsense: 0.005 (R7060)
SMC ADC: 03



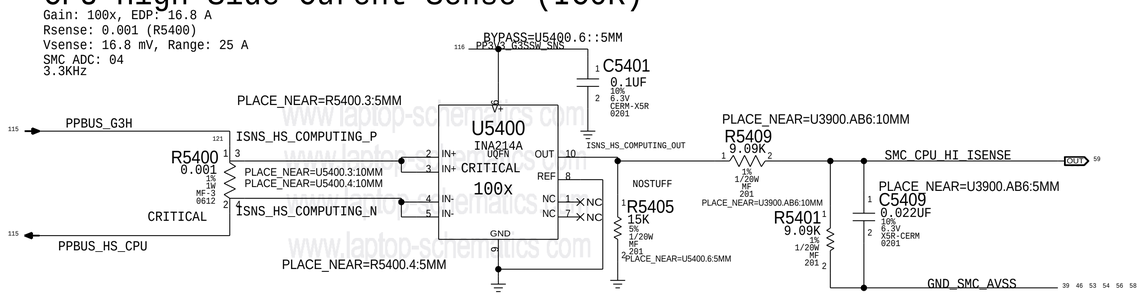

## LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0




## CPU High Side Curent Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 25 A
SMC ADC: 04
3.3KHz




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0008 | 3 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | R5449,R5469,R5419 | | LOADRC:NO |

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors High Side

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
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PAGE 54 OF 200
SHEET 53 OF 131


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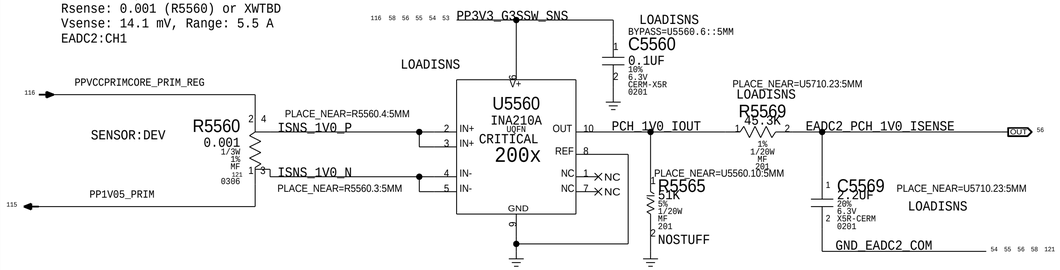
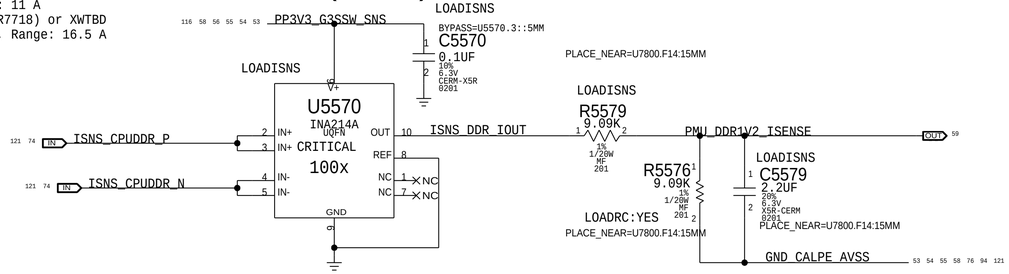
# PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 4.7 A
Rsense: 0.001 (R5560) or XWTBD
Vsense: 14.1 mV, Range: 5.5 A
EADC2:CH1



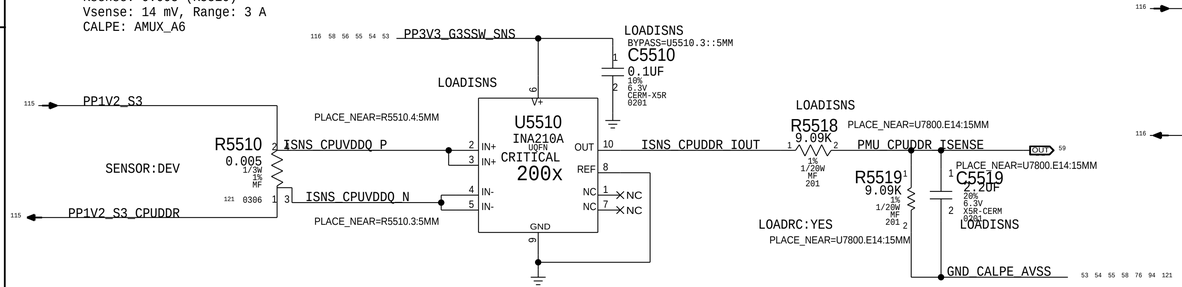

# DDR4 1.2V Current Sense (IM0C)

Gain: 100x, EDP: 11 A
Rsense: 0.002 (R7718) or XWTBD
Vsense: 22.2 mV, Range: 16.5 A
CALPE: AMUX_A7



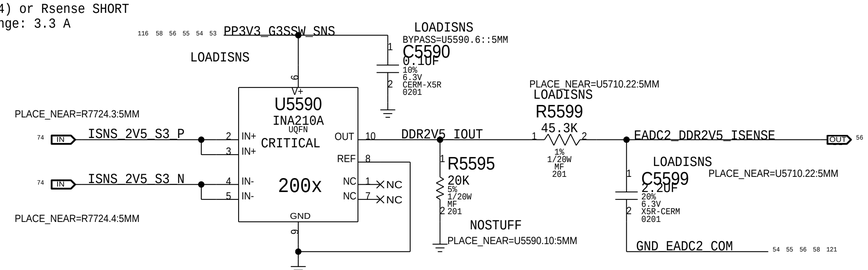

# CPUDDR 1.2V Curent Sense (IMCC)

Gain: 200x, EDP: 2.8 A
Rsense: 0.005 (R5510)
Vsense: 14 mV, Range: 3 A
CALPE: AMUX_A6



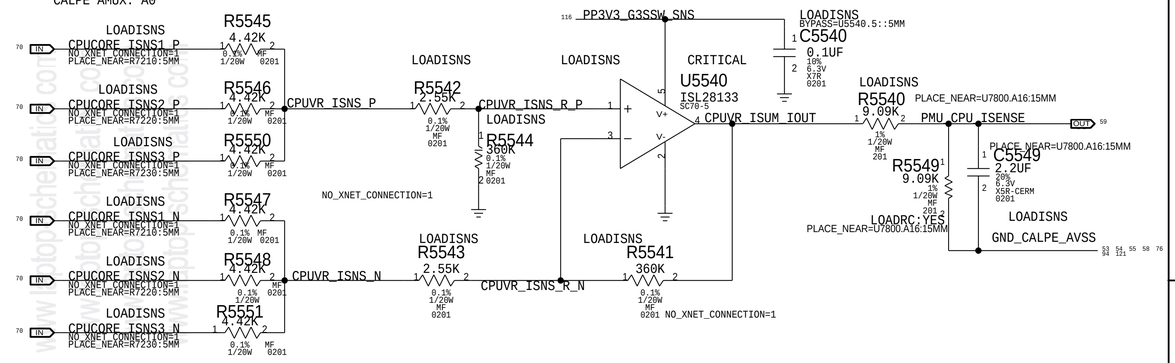

# 2.5V Current Sense (IM1C)

Gain: 200x, EDP: 2.24 A
Rsense: 0.005 (R7724) or Rsense SHORT
Vsense: 11.2 mV, Range: 3.3 A
EADC2: CH0



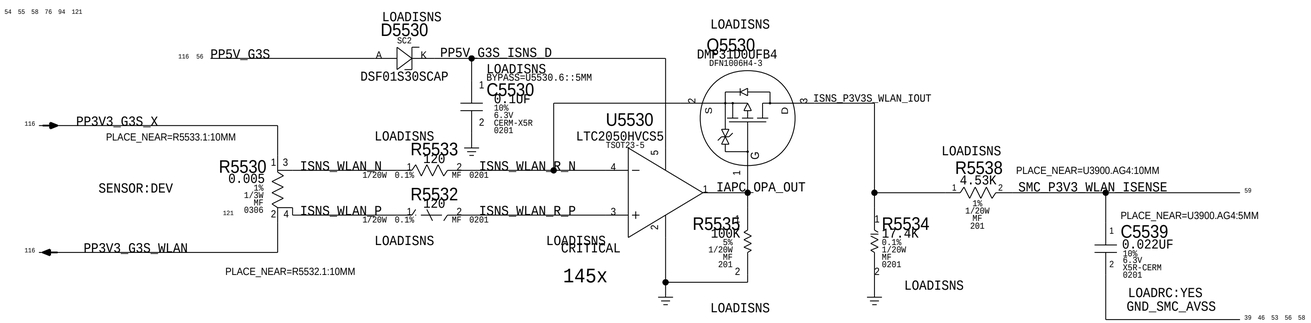

# CPU Core Curent Sense (ICAC)

Gain: 89.48x, EDP: 128 A
Rsense: 3x of 0.00075
R7210,R7220,R7230),Rsum: 0.00025
Vsense:16.75 mV, Range: 134.11 A
CALPE AMUX: A0



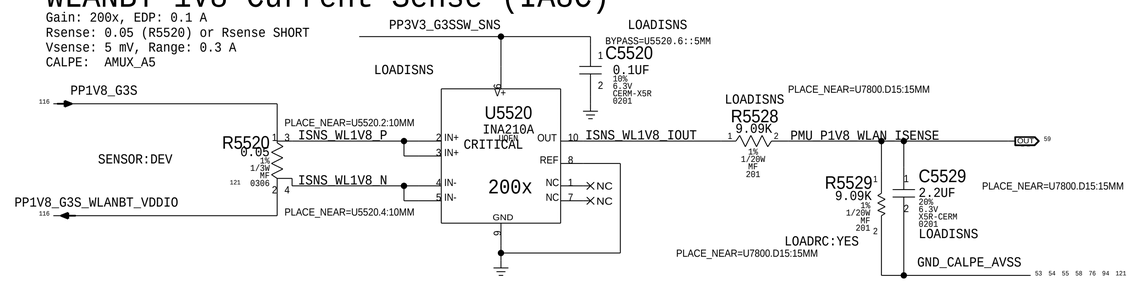

# WLANBT 3V3 Current Sense (IAPC)

Gain: 200x, EDP: 1.5 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 7.5 mV, Range: 1.72 A
SMC: ADC 06




# WLANBT 1V8 Current Sense (IA8C)

Gain: 200x, EDP: 0.1 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 5 mV, Range: 0.3 A
CALPE: AMUX_A5




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0008 | 5 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | R5576,R5519,R5549,C5539,R5529 | | LOADRC:NO |

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Load Side

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 55 OF 200
SHEET: 54 OF 131

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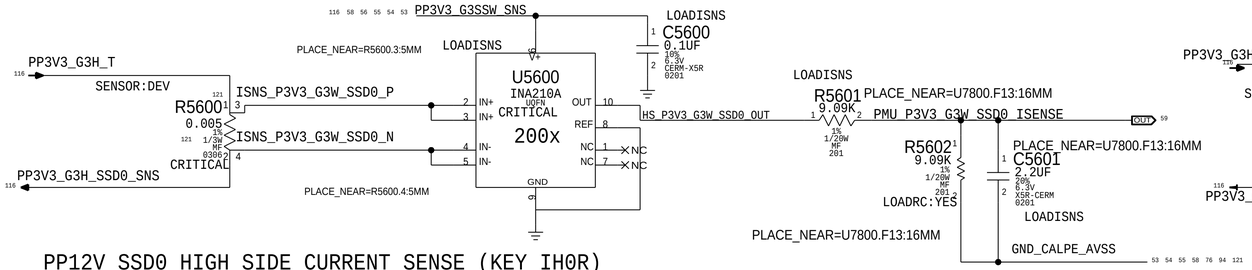
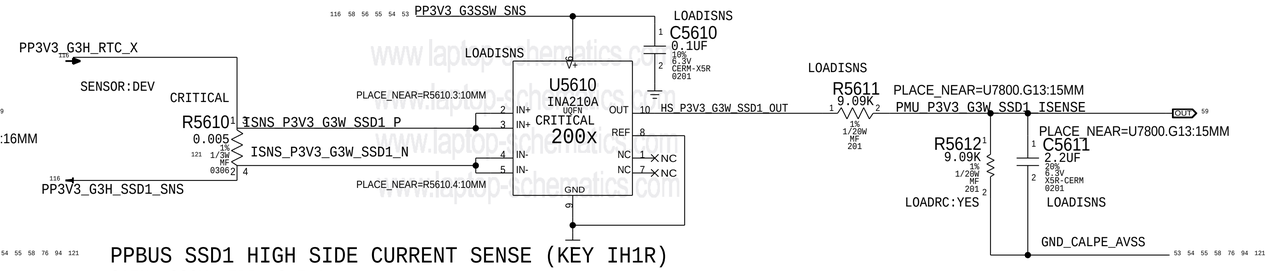
## PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK710) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B3



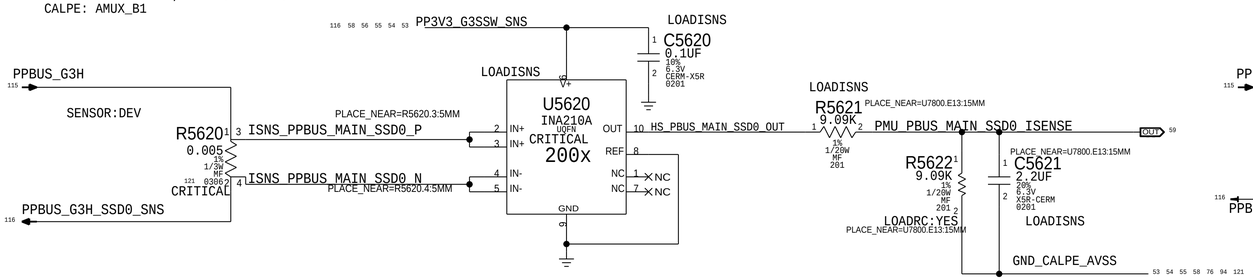

## PP3V3_G3W_SSD1 HIGH SIDE CURRENT SENSE (KEY IH1C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK760) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B4



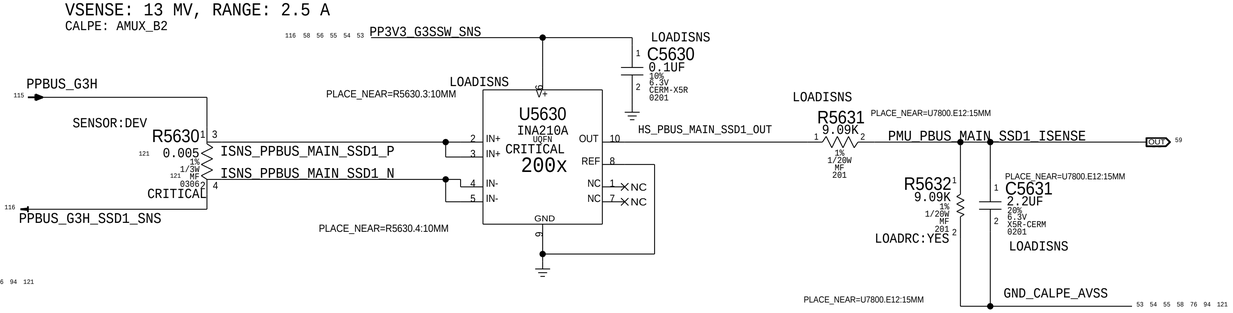

## PP12V SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (RK610) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B1



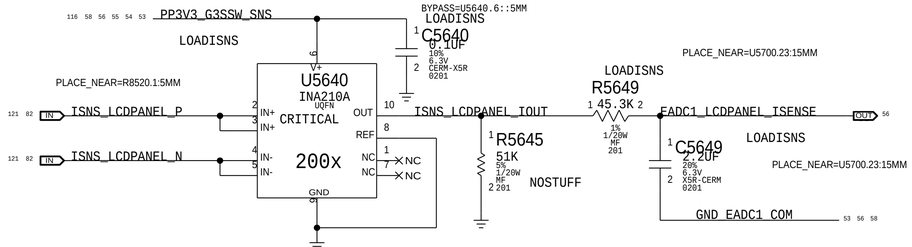

## PPBUS SSD1 HIGH SIDE CURRENT SENSE (KEY IH1R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (R5607) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B2



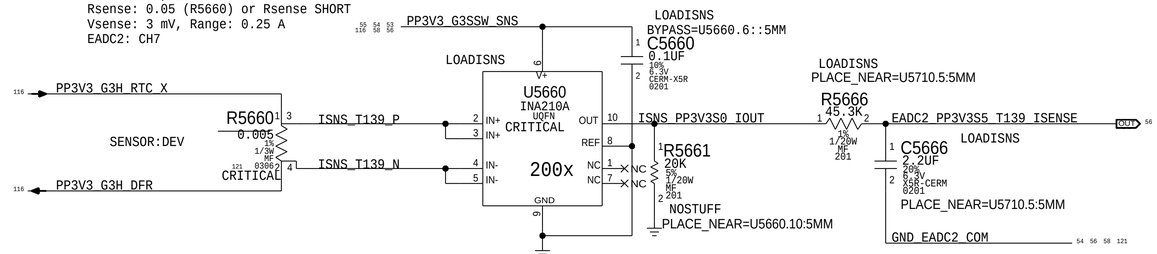

## LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC1: CH1



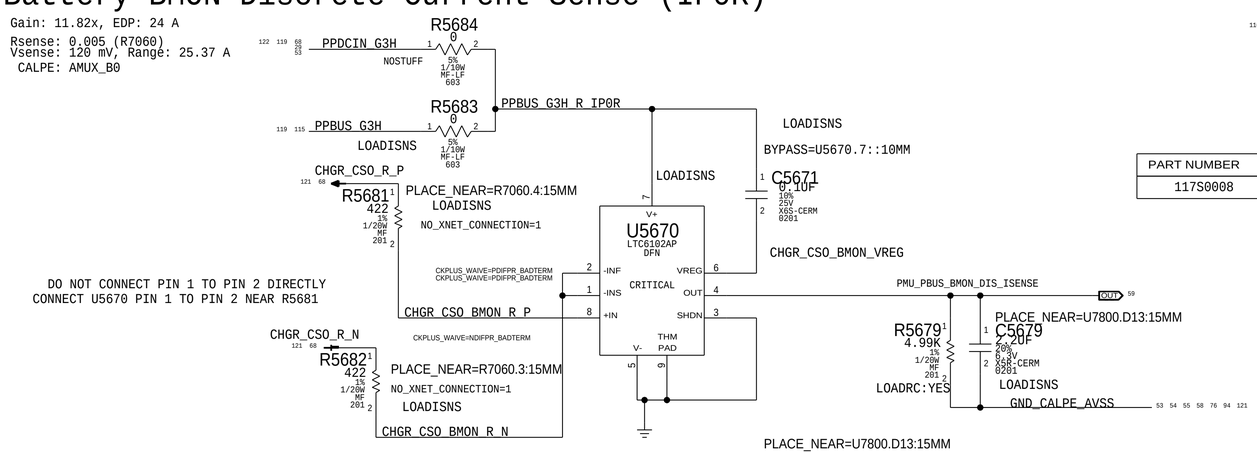

## T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5660) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC2: CH7




## Battery BMON Discrete Current Sense (IP0R)

Gain: 11.82x, EDP: 24 A
Rsense: 0.005 (R7060)
Vsense: 120 mV, Range: 25.37 A
CALPE: AMUX_B0




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0008 | 5 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | R5602,R5612,R5622,R5632,R5679 | | LOADRC:NO |

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors Extended 1

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 56 OF 200
SHEET 55 OF 131

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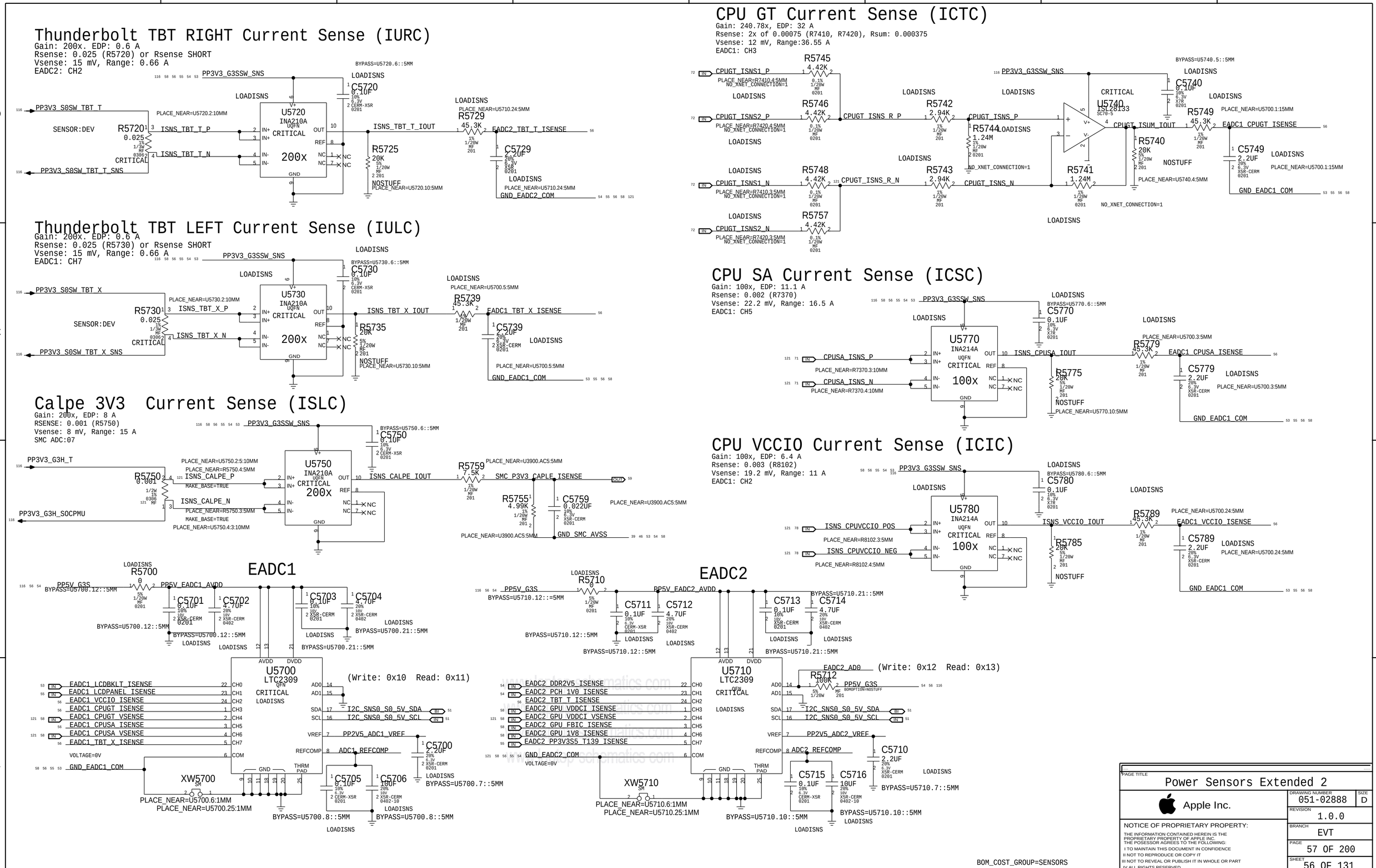


PAGE TITLE
Power Sensors Extended 2

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 57 OF 200
SHEET 56 OF 131

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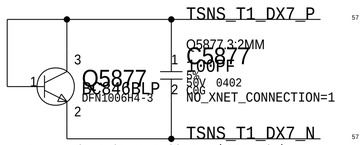
THERMAL DIODE: VRAM PROXIMITY (KEY )

Place Q5877 Bottom,underVRAM shiled can, but not within 2mm of any IC




THERMAL DIODE: GPU ANALOG DIE (KEY TA0P)

Connect GPU Analog Die to U5870 channel 8

## GPU Digital DIE TG0D:

U5880 I2C Address:TMP461 A0->Floating A1->GND 0X92/0X93

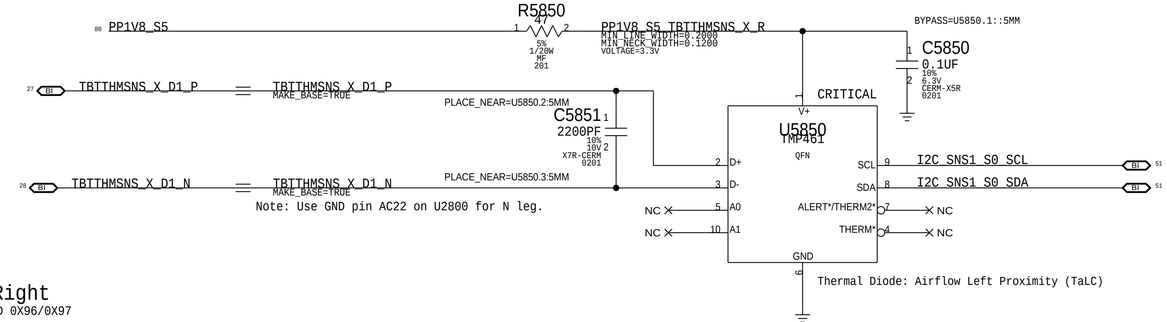
## Thermal Sensor A:

## Thunderbolt Die, Airflow Left

U5850 I2C Address:TMP461 A1->Floating A0->Floating 0X98/0X99

## Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.




Note: Use GND pin AC22 on U2800 for N leg.

Thermal Diode: Airflow Left Proximity (TaLC)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

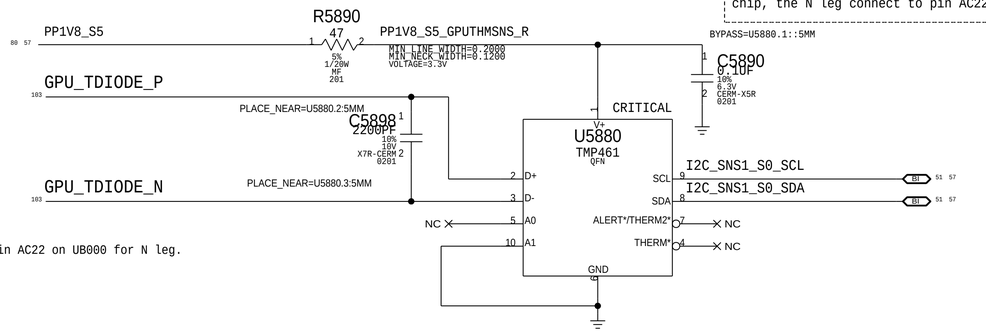
## Thermal Sensor C:

## Thunderbolt Die, Air Flow Right

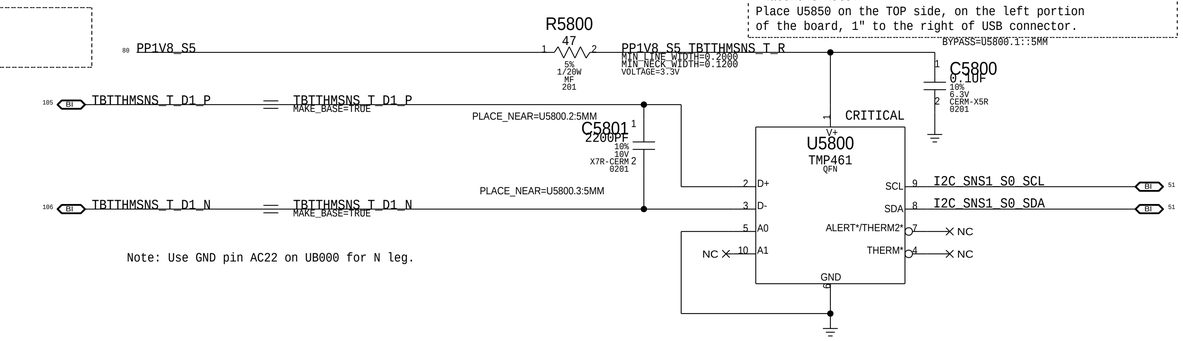
U5800 I2C Address:TMP461 A1->Floating A0->GND 0X96/0X97

## Thermal Diode: TBT Die (TTRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.




Note: Use GND pin AC22 on UB000 for N leg.



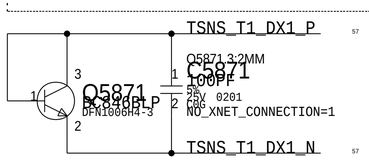

Note: Use GND pin AC22 on UB000 for N leg.

Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

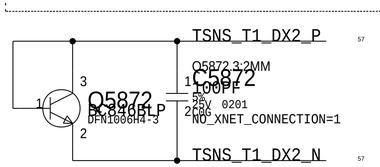
THERMAL DIODE: CPU PROX (KEY TC0P)

Placement Note:
Place Q5871 under the CPU ON BOTTOM SIDE



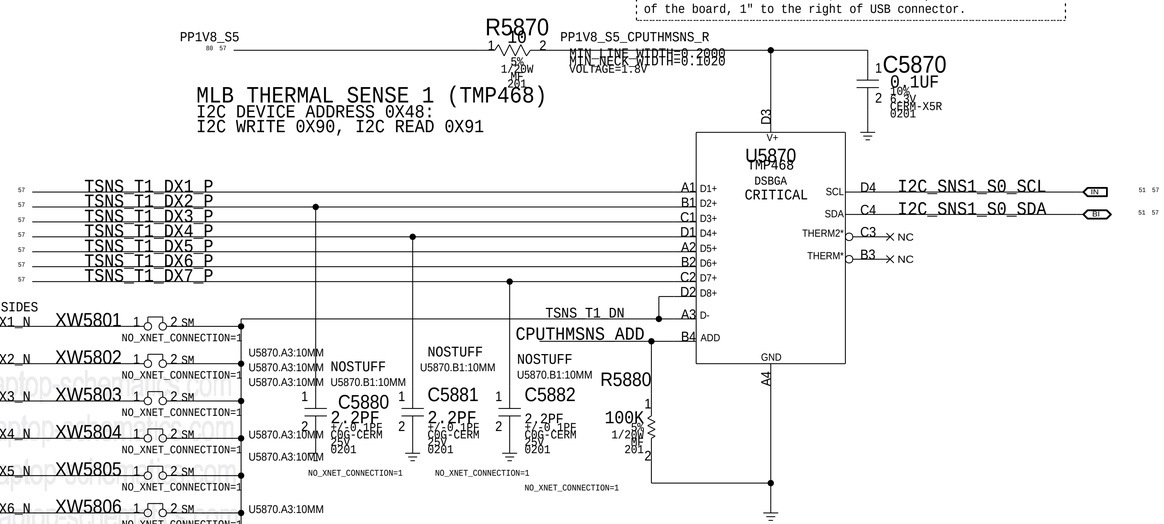

THERMAL DIODE: FIN STACK LEFT (KEY TH2H)

Placement Note:
Place Q5872,AIRFLOW THERMAL INDICATOR,ABOVETHE X100, ON THE TOP SIDE




## MLB THERMAL SENSE 1 (TMP468)

I2C DEVICE ADDRESS 0X48:
I2C WRITE 0X90, I2C READ 0X91

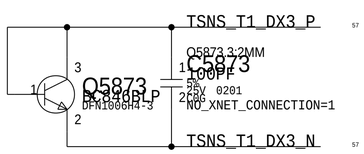



MLB PROX 2 is read from the on-chip temp sensors U5870

Place U5870 near Calpe (U7800)

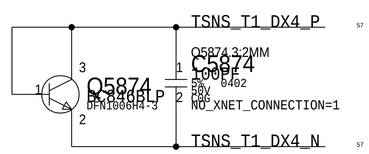
THERMAL DIODE: FIN STACK RIGHT (KEY TH1H)

Placement Note:
Place Q5873 AT THE CORNER NEAR RIGHT FAN, ON THE TOP SIDE



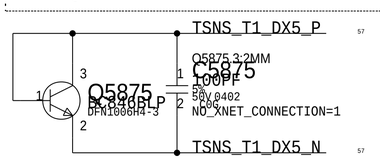

THERMAL DIODE: Memory Proximity (KEY TM0P)

Place Q5874 between two rows of Memory devices, between channel A and CHANNEHL b PN BOTTOM SIDES



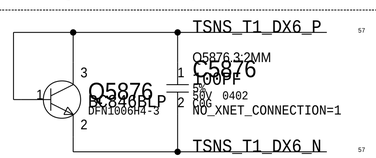

THERMAL DIODE: X100 PROXIMITY (KEY TW0P)

Place Q5875 near X100 on bottom




THERMAL DIODE: GPU PROXIMITY(KEY )

Place Q5876 near GPU, Top side




BOM_COST_GROUP=SENSORS

| | |
|---|---|
| PAGE TITLE | Thermal Sensors |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
| | REVISION 1.0.0 |
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| | PAGE 58 OF 200 |
| | SHEET 57 OF 131 |

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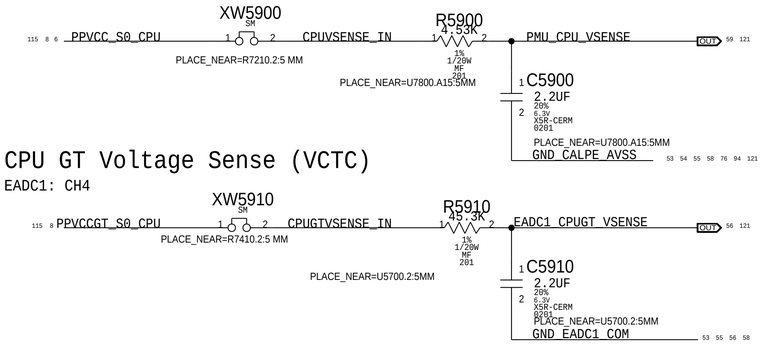
# GPU SENSORS

## CPU Core Voltage Sense (VCAC)

CALPE : AMUX-A1



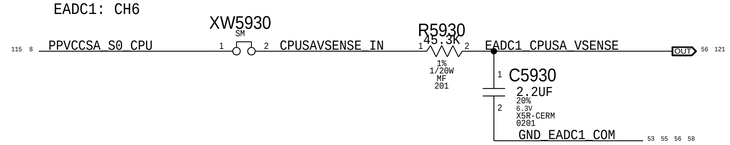

## CPU GT Voltage Sense (VCTC)

EADC1: CH4



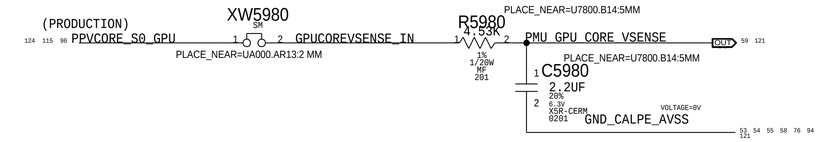

## CPU SA Voltage Sense (VCSC)

EADC1: CH6



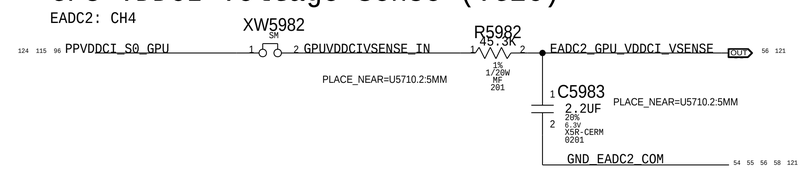

## GPU CORE Voltage Sense (VG0C)

CALPE: AMUX-A3




## GPU VDDCI Voltage Sense (VG2C)

EADC2: CH4

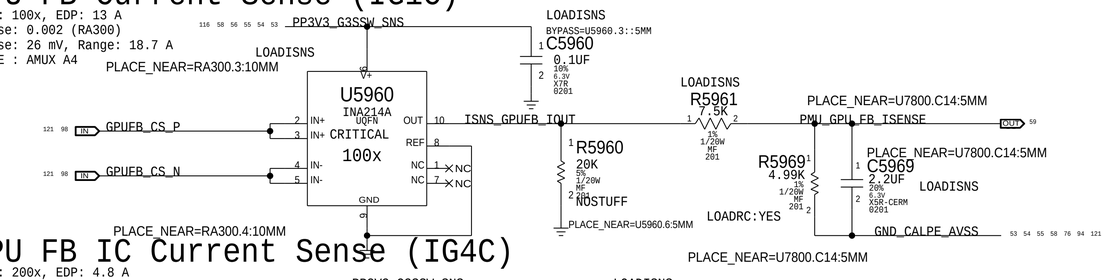



## GPU CORE Current Sense (IG0C)
## no longer lives on this page
## it's merged with the PCC circuit
## on CSA 99

Gain: 154.87x, EDP: 78 A
Rsense: 3X OF 0.00075 (RA651,RA641,RA346)
Vsense: 19.5 mV, Range: 109 A
CALPE : AMUX A2

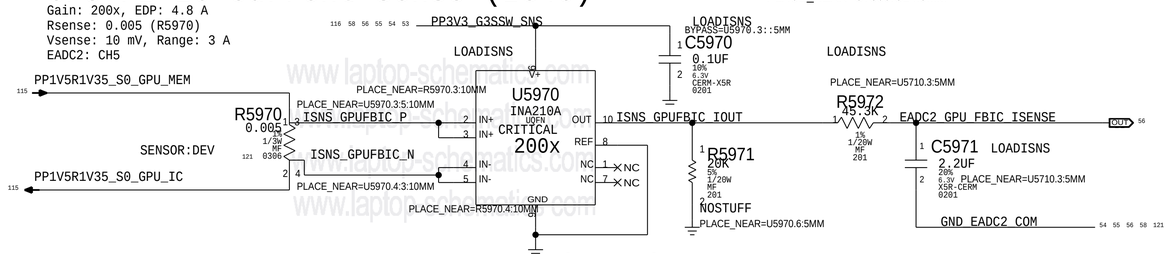
## GPU FB Current Sense (IG1C)

Gain: 100x, EDP: 13 A
Rsense: 0.002 (RA300)
Vsense: 26 mV, Range: 18.7 A
CALPE : AMUX A4



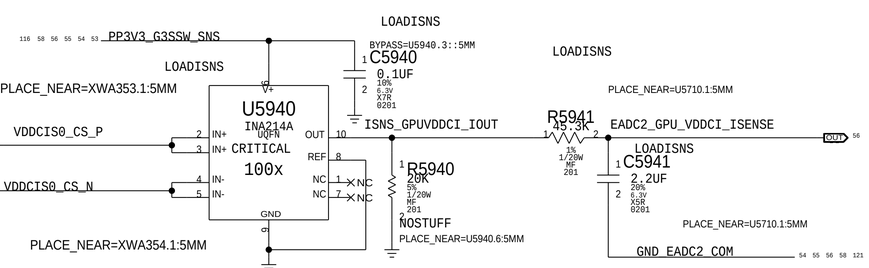

## GPU FB IC Current Sense (IG4C)

Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
EADC2: CH5




## GPU VDDCI Current Sense (IG2C)

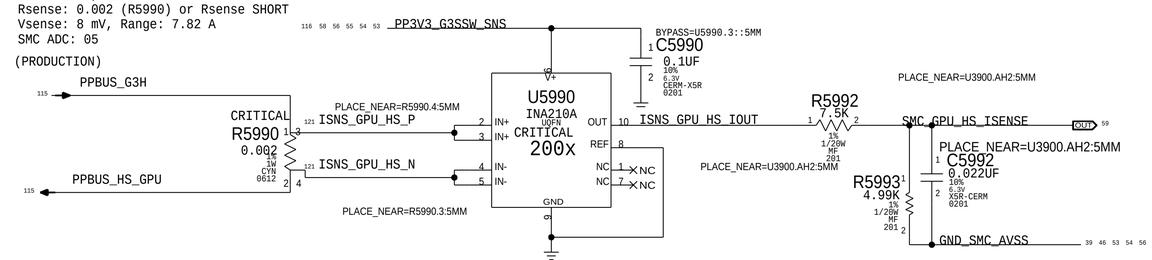
Gain: 100x, EDP: 10 A
Rsense: 0.003 (RA368)
Vsense: 20 mV, Range: 16.5 A
EADC2: CH3




## GPU HIGH SIDE Current Sense (IG0R)

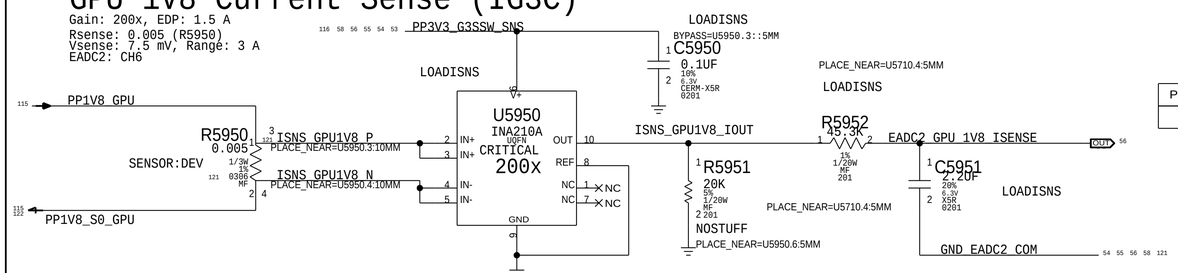
Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.82 A
SMC ADC: 05

(PRODUCTION)




## GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 1.5 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
EADC2: CH6




| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0008 | 1 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | R5969 | | LOADRC:NO |

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensor Extended 3

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PAGE 59 OF 200
SHEET 58 OF 131


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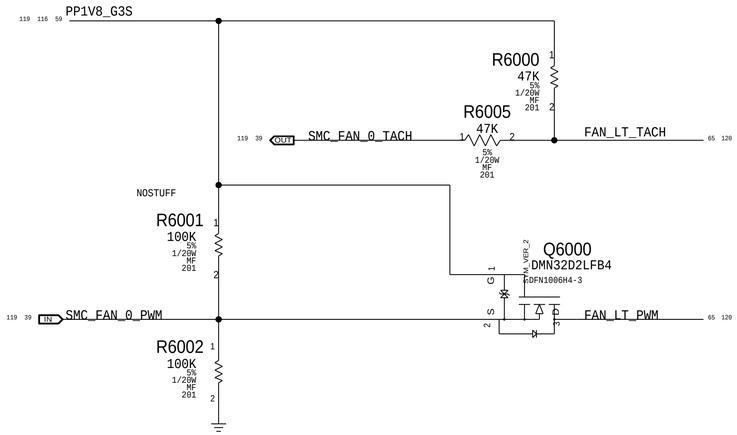
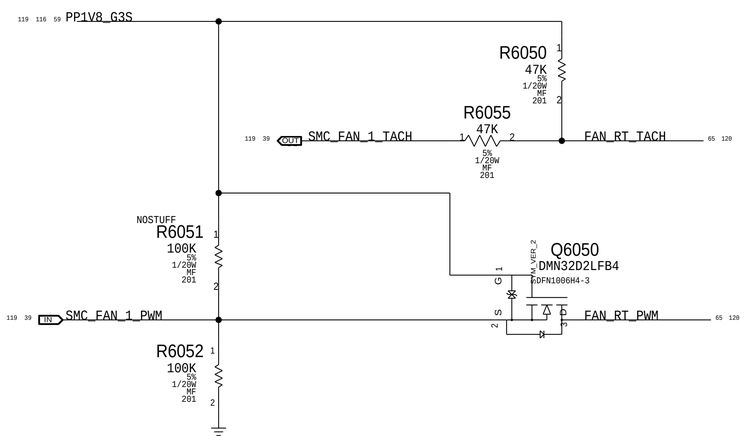
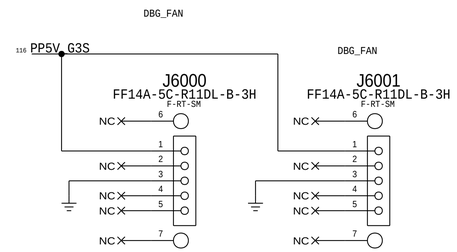
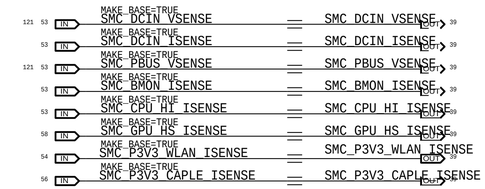
# FAN CONNECTOR



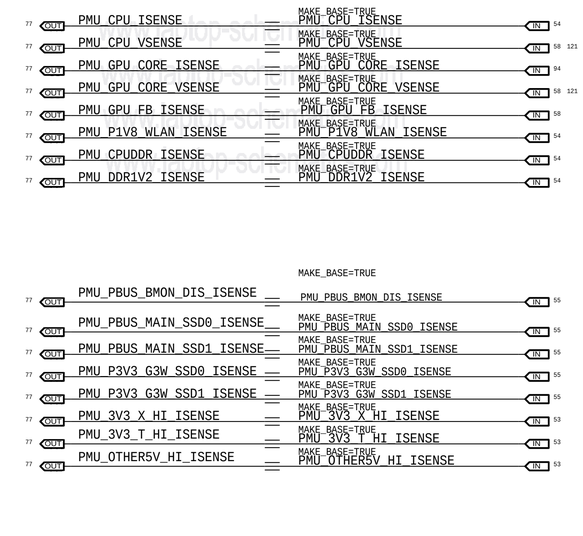




## H9M SMC ADC Assignments




## CALPE AMUX Assignments




BOM_COST_GROUP=FAN

PAGE TITLE
Fans/SMC/AMUX Support

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SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 60 OF 200
SHEET 59 OF 131

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DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
Audio Placeholder

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SIZE D
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BRANCH EVT
PAGE 62 OF 200
SHEET 60 OF 131

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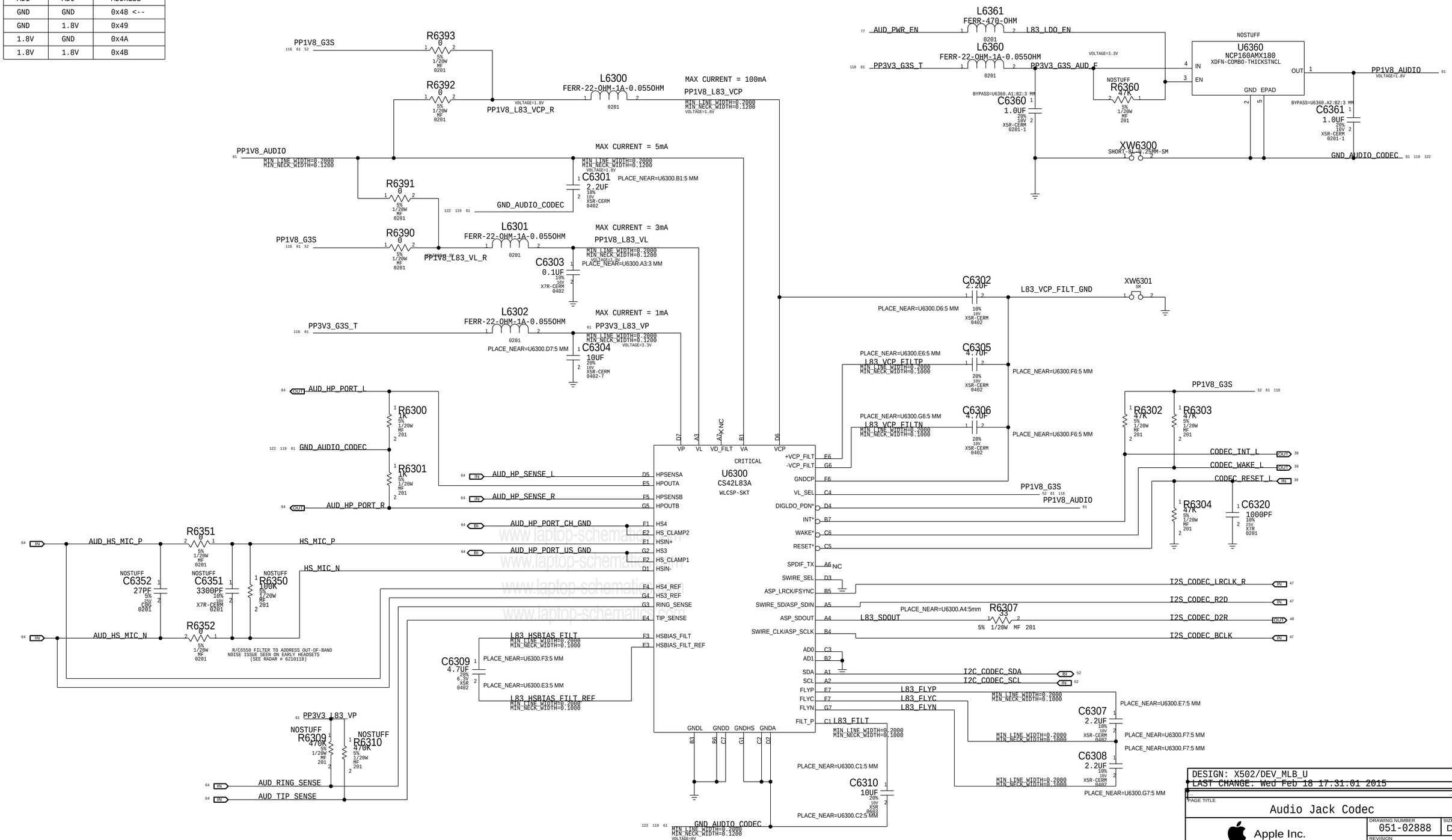
| AUDIO JACK CODEC I2C ADDRESS | | |
|---|---|---|
| AD1 | AD0 | ADDRESS |
| GND | GND | 0x48 <-- |
| GND | 1.8V | 0x49 |
| 1.8V | GND | 0x4A |
| 1.8V | 1.8V | 0x4B |

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DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:31.01 2015

PAGE TITLE
Audio Jack Codec

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BRANCH EVT
PAGE 63 OF 200
SHEET 61 OF 131

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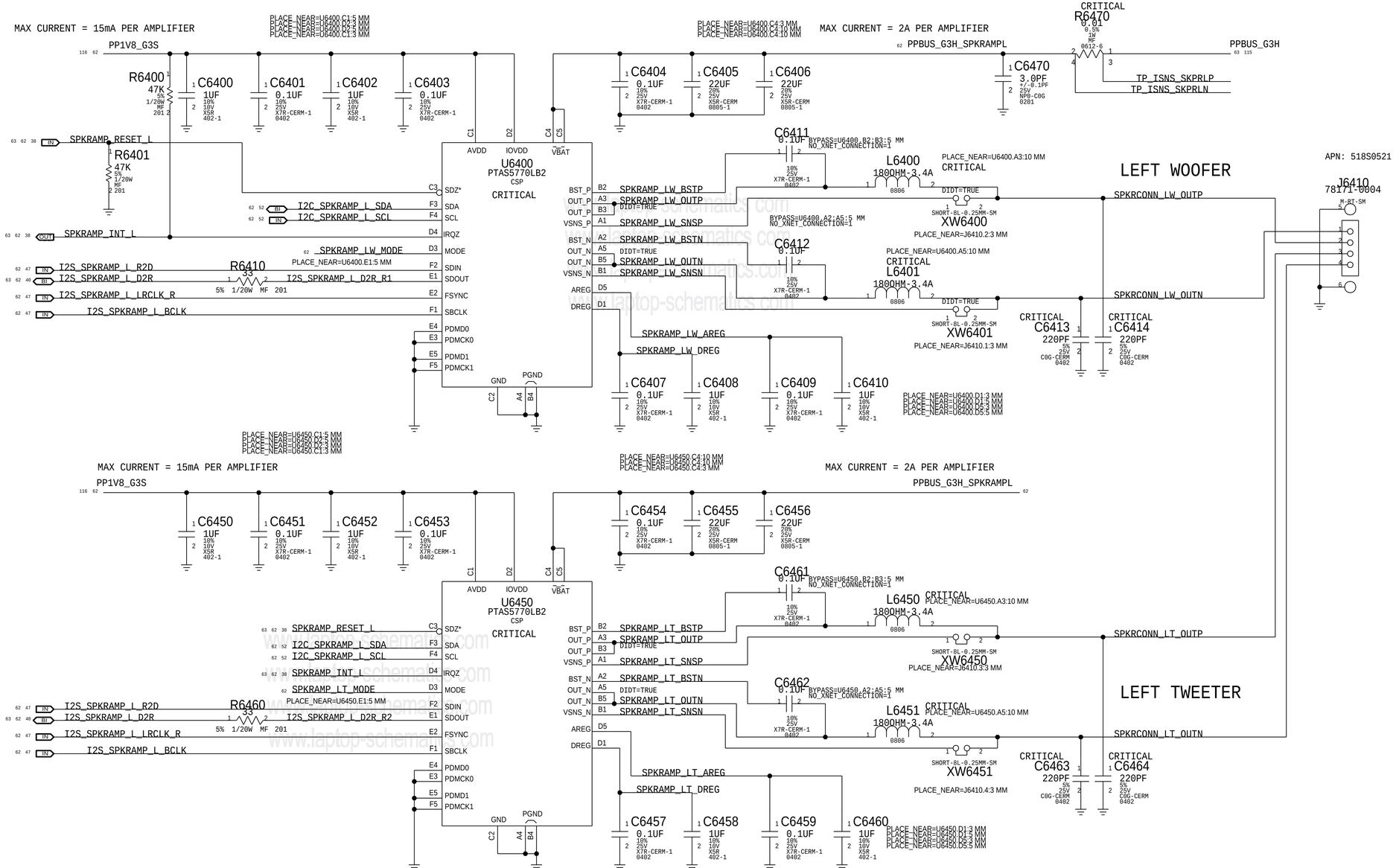
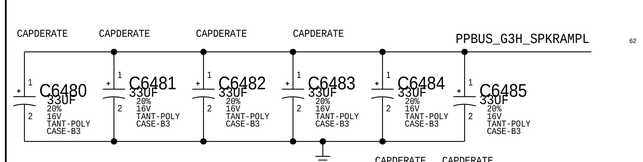
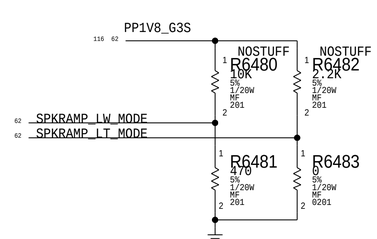
# 2X MONO SPEAKER LEFT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS




LEFT BULK CAPACITANCE




I2C ADDRESS

| MODE PIN | 7-BIT | CHANNEL |
|---|---|---|
| GND | 0x31 | L TW |
| 470 to GND | 0x32 | L WF |
| 470 to IOVDD | 0x33 | R TW |
| 2K2 to GND | 0x34 | R WF |
| 2K2 to IOVDD | 0x35 | |
| 10k to GND | 0x36 | |
| 10k to IOVDD | 0x37 | |
| 47k to IOVDD | 0x38 | |

BOM_COST_GROUP=AUDIO

SYNC_MASTER=TROY SYNC_DATE=12/11/2017

PAGE TITLE: Audio Left Amplifiers

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 64 OF 200
SHEET: 62 OF 131

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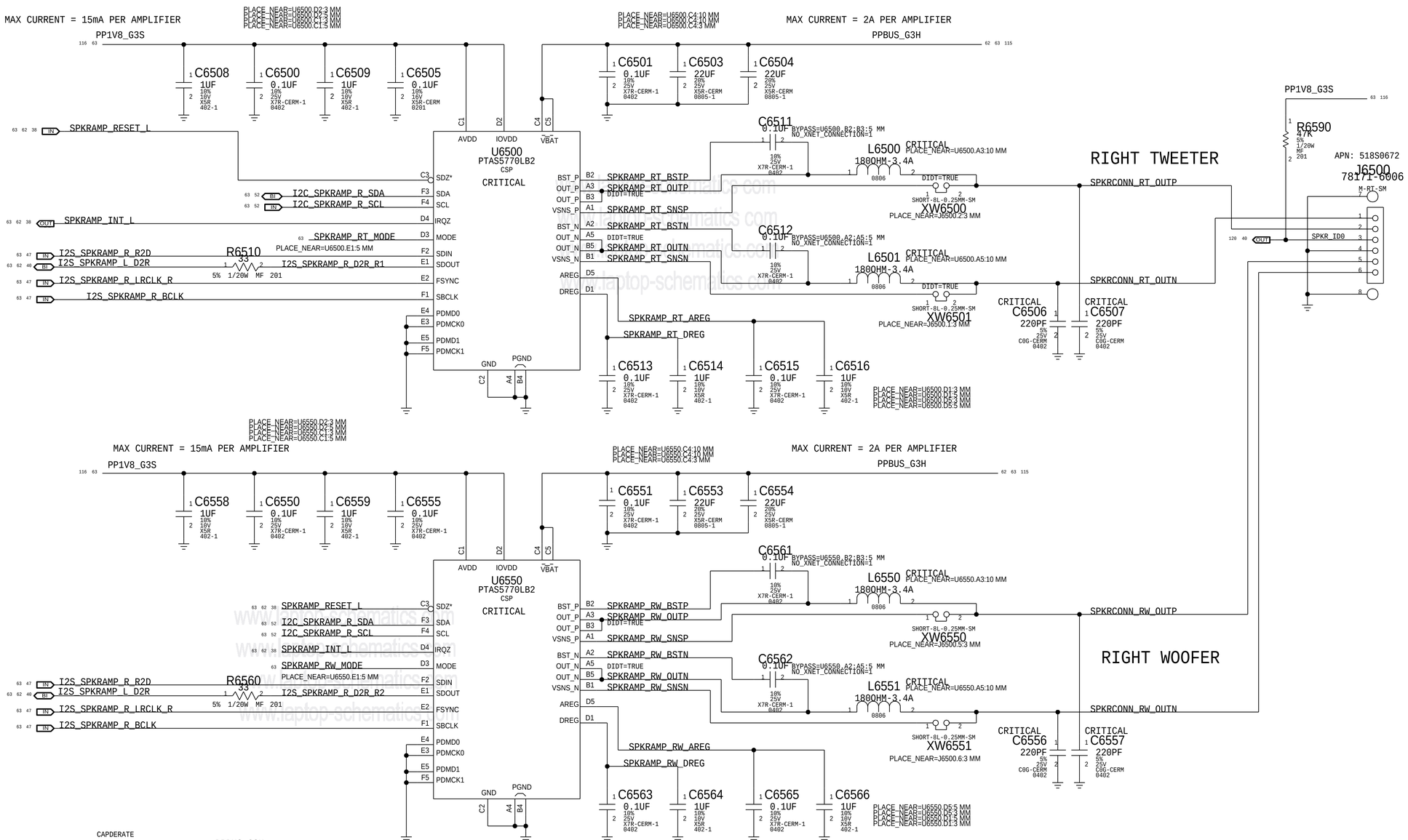
# 2X MONO SPEAKER RIGHT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS




I2C ADDRESS

| MODE PIN | 7-BIT | CHANNEL |
|---|---|---|
| GND | 0x31 | L TW |
| 470 to GND | 0x32 | L WF |
| 470 to IOVDD | 0x33 | R TW |
| 2K2 to GND | 0x34 | R WF |
| 2K2 to IOVDD | 0x35 | |
| 10k to GND | 0x36 | |
| 10k to IOVDD | 0x37 | |
| 47k to IOVDD | 0x38 | |

BOM_COST_GROUP=AUDIO

PAGE TITLE: Audio Right Amplifiers

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 65 OF 200
SHEET: 63 OF 131

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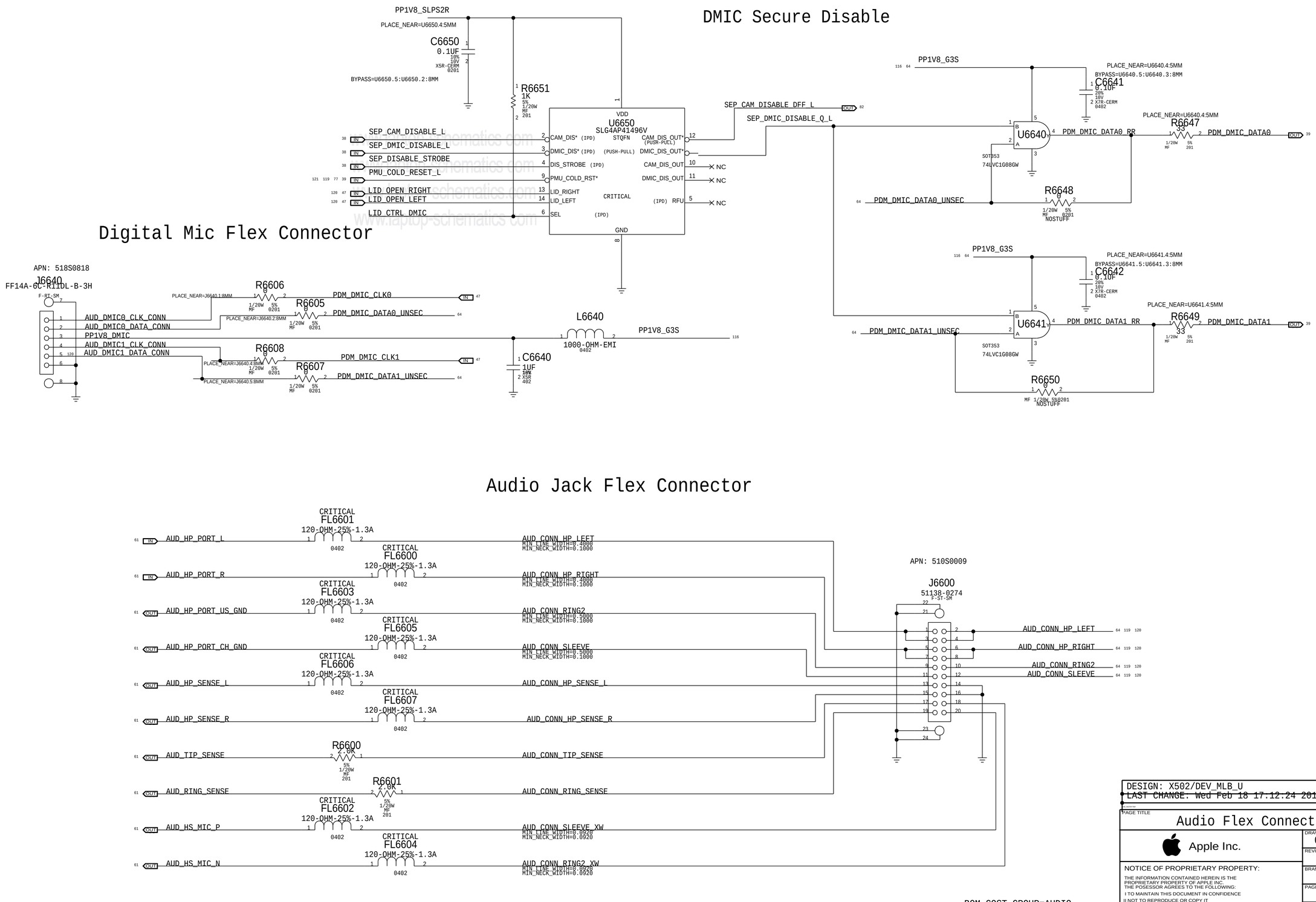


DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
Audio Flex Connectors

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 66 OF 200
SHEET 64 OF 131

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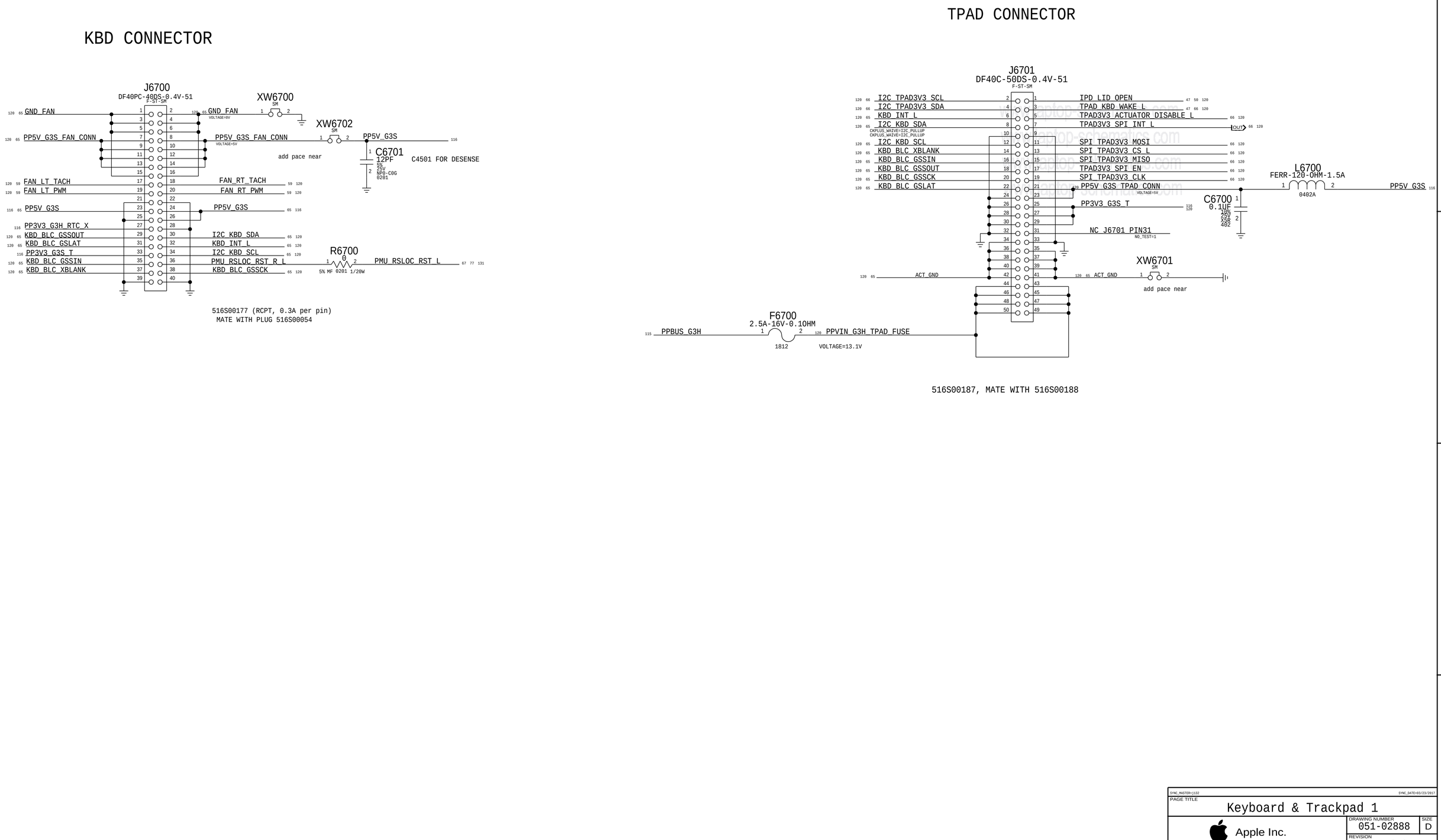


BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=1332 SYNC_DATE=03/23/2017

PAGE TITLE

Keyboard & Trackpad 1

Apple Inc.

DRAWING NUMBER 051-02888

SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 67 OF 200

SHEET 65 OF 131

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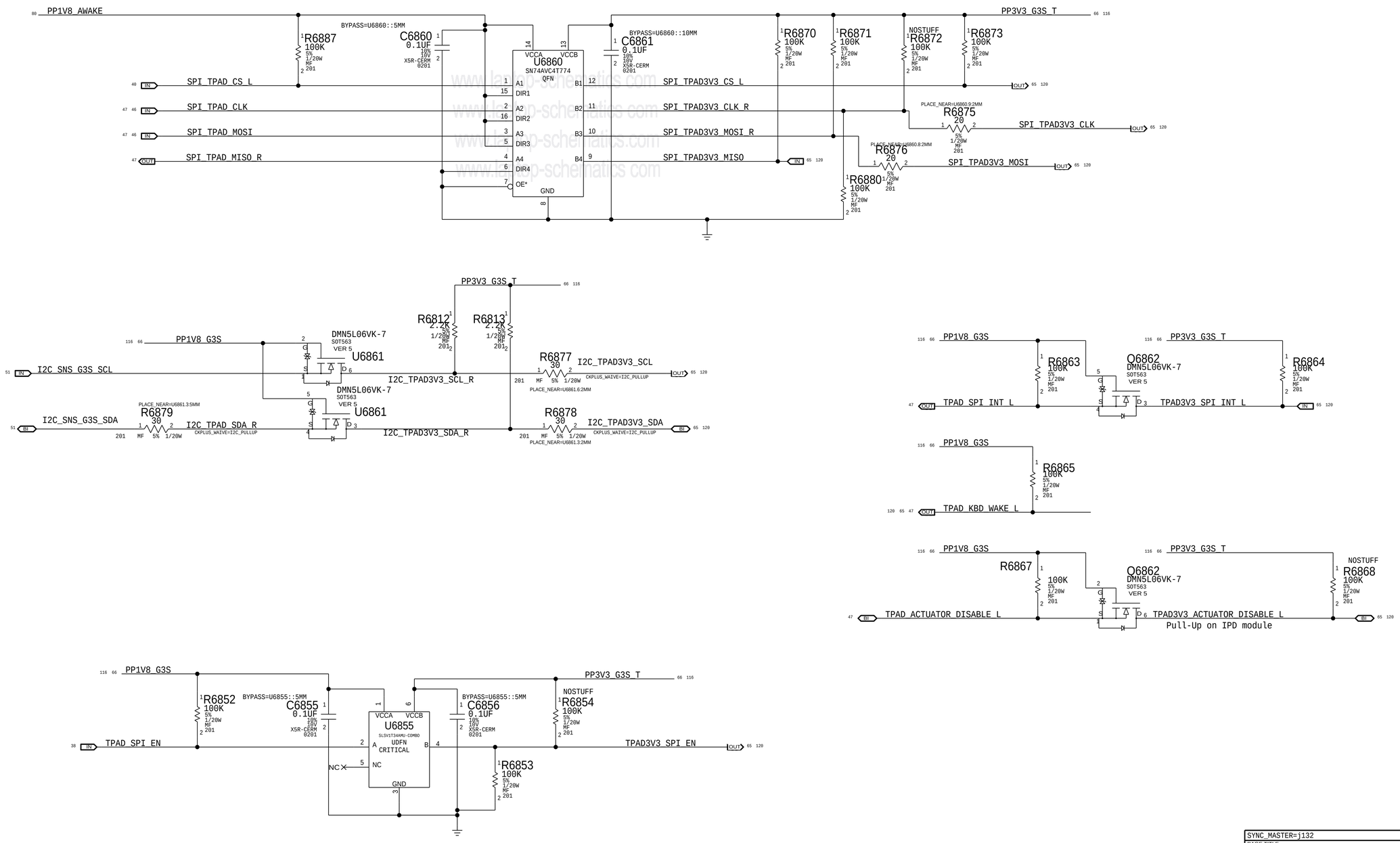
# Trackpad Level Shifting




BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=j132 SYNC_DATE=03/23/2017

PAGE TITLE
Keyboard & Trackpad 2

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 68 OF 200

SHEET 66 OF 131

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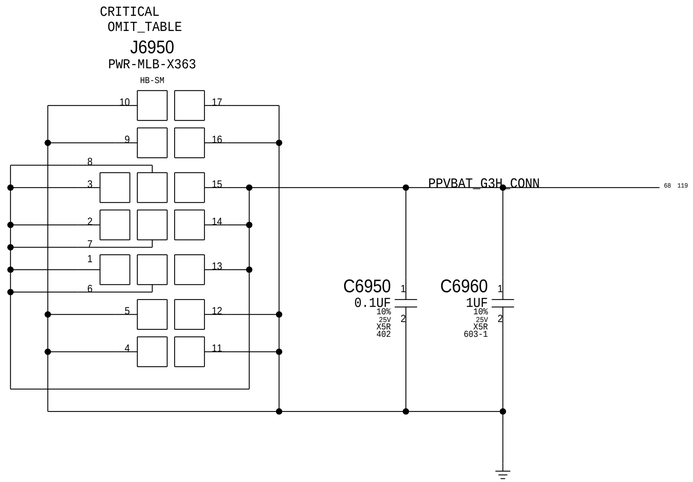
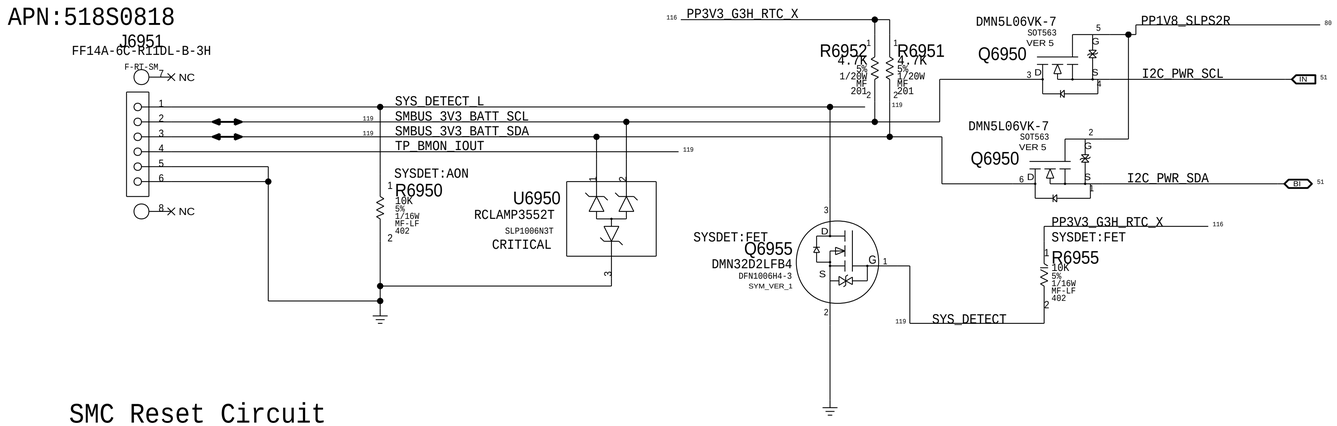
J80 Battery Hotbar Flex Pads 998-03902
Flex Pad TO MLB 998-03780.




BMU POWER FLEX HOTBAR'd TO THE MLB:

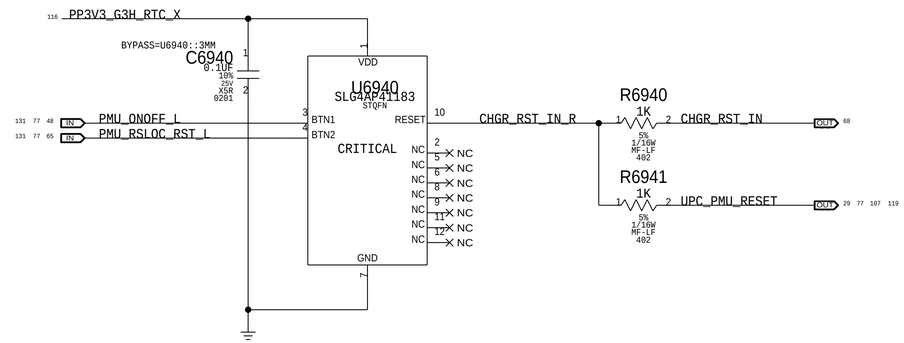
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 632-00862 | 1 | PCBA,FLEX,BMU PWR,X363 | J6950 | CRITICAL | |

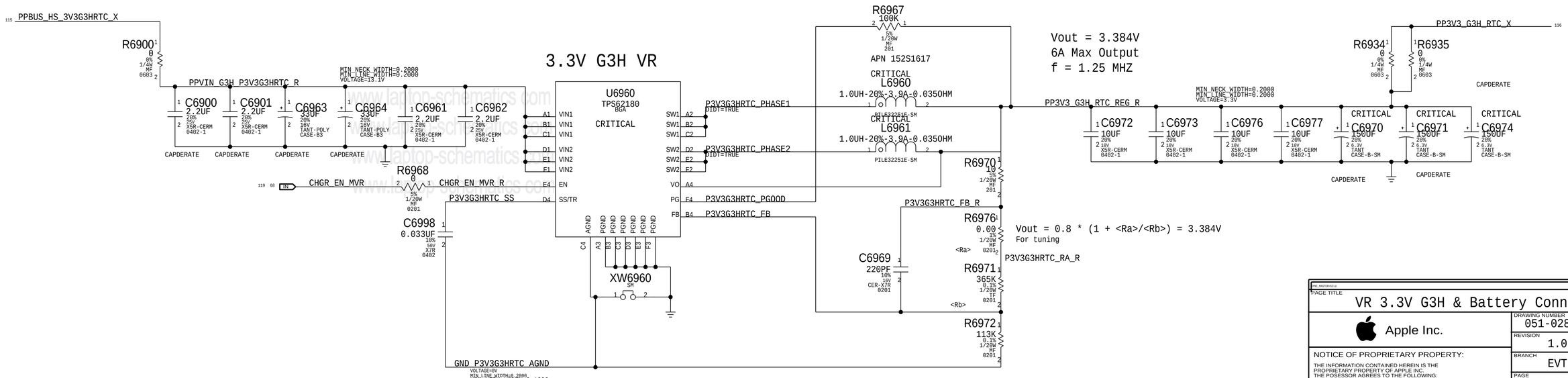
APN:518S0818




## SMC Reset Circuit

Right Shift & Left Option Control
followed by ON OFF button press.




BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
VR 3.3V G3H & Battery Conn

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 69 OF 200
SHEET 67 OF 131

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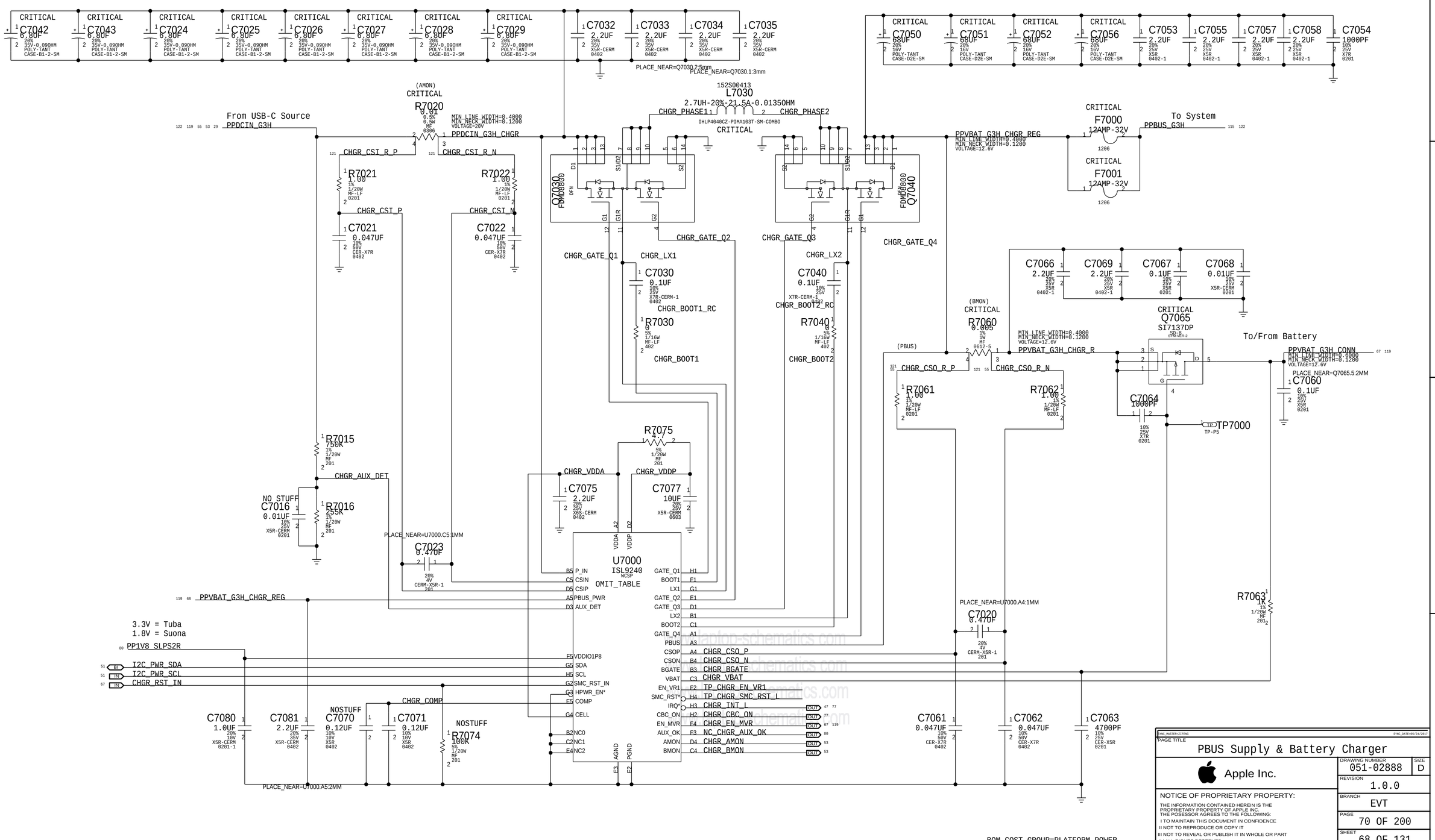
CRITICAL C7042 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7043 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7024 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7025 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7026 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7027 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7028 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
CRITICAL C7029 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM
C7032 2.2UF 20% 35V X5R-CERM 0402
C7033 2.2UF 20% 35V X5R-CERM 0402
C7034 2.2UF 20% 35V X5R-CERM 0402
C7035 2.2UF 20% 35V X5R-CERM 0402
PLACE_NEAR=Q7030.2:5mm
PLACE_NEAR=Q7030.1:3mm
CRITICAL C7050 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7051 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7052 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7056 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7053 2.2UF 20% 25V X5R 0402-1
C7055 2.2UF 20% 25V X5R 0402-1
C7057 2.2UF 20% 25V X5R 0402-1
C7058 2.2UF 20% 25V X5R 0402-1
C7054 1000PF 10% 25V X7R 0201
(AMON)
CRITICAL
R7020 0.01 0.5% 0.5W MF 0306
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V
From USB-C Source
PPDCIN_G3H
PPDCIN_G3H_CHGR
CHGR_CSI_R_P
CHGR_CSI_R_N
R7021 1.00 1% 1/20W MF-LF 0201
R7022 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_P
CHGR_CSI_N
C7021 0.047UF 10% 50V CER-X7R 0402
C7022 0.047UF 10% 50V CER-X7R 0402
152S00413
L7030
2.7UH-20%-21.5A-0.01350HM
IHLP4040CZ-PIMA103T-SM-COMBO
CHGR_PHASE1
CHGR_PHASE2
CRITICAL
Q7030 FDMC8800 DFN
Q7040 FDMC8800
CHGR_GATE_Q1
CHGR_GATE_Q2
CHGR_GATE_Q3
CHGR_GATE_Q4
CHGR_LX1
CHGR_LX2
C7030 0.1UF 10% 25V X7R-CERM-1 0402
C7040 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC
CHGR_BOOT2_RC
R7030 0 5% 1/16W MF-LF 402
R7040 0 5% 1/16W MF-LF 402
CHGR_BOOT1
CHGR_BOOT2
PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
CRITICAL F7000 12AMP-32V 1206
CRITICAL F7001 12AMP-32V 1206
To System
PPBUS_G3H
C7066 2.2UF 20% 25V X5R 0402-1
C7069 2.2UF 20% 25V X5R 0402-1
C7067 0.1UF 10% 25V X5R 0201
C7068 0.01UF 10% 25V X5R-CERM 0201
(BMON)
CRITICAL
R7060 0.005 1% 1W MF 0612-5
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PPVBAT_G3H_CHGR_R
CRITICAL Q7065 SI7137DP SO-8
To/From Battery
PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PLACE_NEAR=Q7065.5:2MM
C7060 0.1UF 10% 25V X5R 0201
(PBUS)
CHGR_CSO_R_P
CHGR_CSO_R_N
R7061 1.00 1% 1/20W MF-LF 0201
R7062 1.00 1% 1/20W MF-LF 0201
C7064 1000PF 10% 25V X7R 0201
TP7000 TP-P5
R7015 750K 1% 1/20W MF 201
CHGR_AUX_DET
NO_STUFF
C7016 0.01UF 10% 25V X5R-CERM 0201
R7016 255K 1% 1/20W MF 201
R7075 4.7 5% 1/20W MF 201
CHGR_VDDA
CHGR_VDDP
C7075 2.2UF 20% 25V X6S-CERM 0402
C7077 10UF 20% 25V X5R-CERM 0603
PLACE_NEAR=U7000.C5:1MM
C7023 0.47UF 20% 4V CERM-X5R-1 201
U7000 ISL9240 WCSP
OMIT_TABLE
VDDA_A2
VDDP_D2
B5 P_IN
C5 CSIN
D5 CSIP
A5 PBUS_PWR
D3 AUX_DET
E5 VDDIO1P8
G5 SDA
H5 SCL
G2 SMC_RST_IN
G3 HPWR_EN*
E5 COMP
G4 CELL
B2 NC0
C2 NC1
E4 NC2
E3 AGND
E2 PGND
GATE_Q1 H1
BOOT1 F1
LX1 G1
GATE_Q2 E1
GATE_Q3 D1
LX2 B1
BOOT2 C1
GATE_Q4 A1
PBUS A3
CSOP A4 CHGR_CSO_P
CSON B4 CHGR_CSO_N
BGATE B3 CHGR_BGATE
VBAT C3 CHGR_VBAT
EN_VR1 F2 TP_CHGR_EN_VR1
SMC_RST* H4 TP_CHGR_SMC_RST_L
IRQ* H3 CHGR_INT_L
CBC_ON H2 CHGR_CBC_ON
EN_MVR F4 CHGR_EN_MVR
AUX_OK F3 NC_CHGR_AUX_OK
AMON D4 CHGR_AMON
BMON C4 CHGR_BMON
PPVBAT_G3H_CHGR_REG
3.3V = Tuba
1.8V = Suona
PP1V8_SLPS2R
I2C_PWR_SDA
I2C_PWR_SCL
CHGR_RST_IN
C7080 1.0UF 20% 10V X5R-CERM 0201-1
C7081 2.2UF 20% 35V X5R-CERM 0402
NOSTUFF
C7070 0.12UF 10% 16V X5R 0402
C7071 0.12UF 10% 16V X5R 0402
CHGR_COMP
NOSTUFF
R7074 100K 5% 1/20W MF 201
PLACE_NEAR=U7000.A5:2MM
PLACE_NEAR=U7000.A4:1MM
C7020 0.47UF 20% 4V CERM-X5R-1 201
C7061 0.047UF 10% 50V CER-X7R 0402
C7062 0.047UF 10% 50V CER-X7R 0402
C7063 4700PF 10% 25V CER-X5R 0201
R7063 1K 1% 1/20W MF 201
BOM_COST_GROUP=PLATFORM POWER
SYNC_MASTER=J2FH96
SYNC_DATE=05/24/2017
PAGE TITLE
PBUS Supply & Battery Charger
Apple Inc.
DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 70 OF 200
SHEET 68 OF 131
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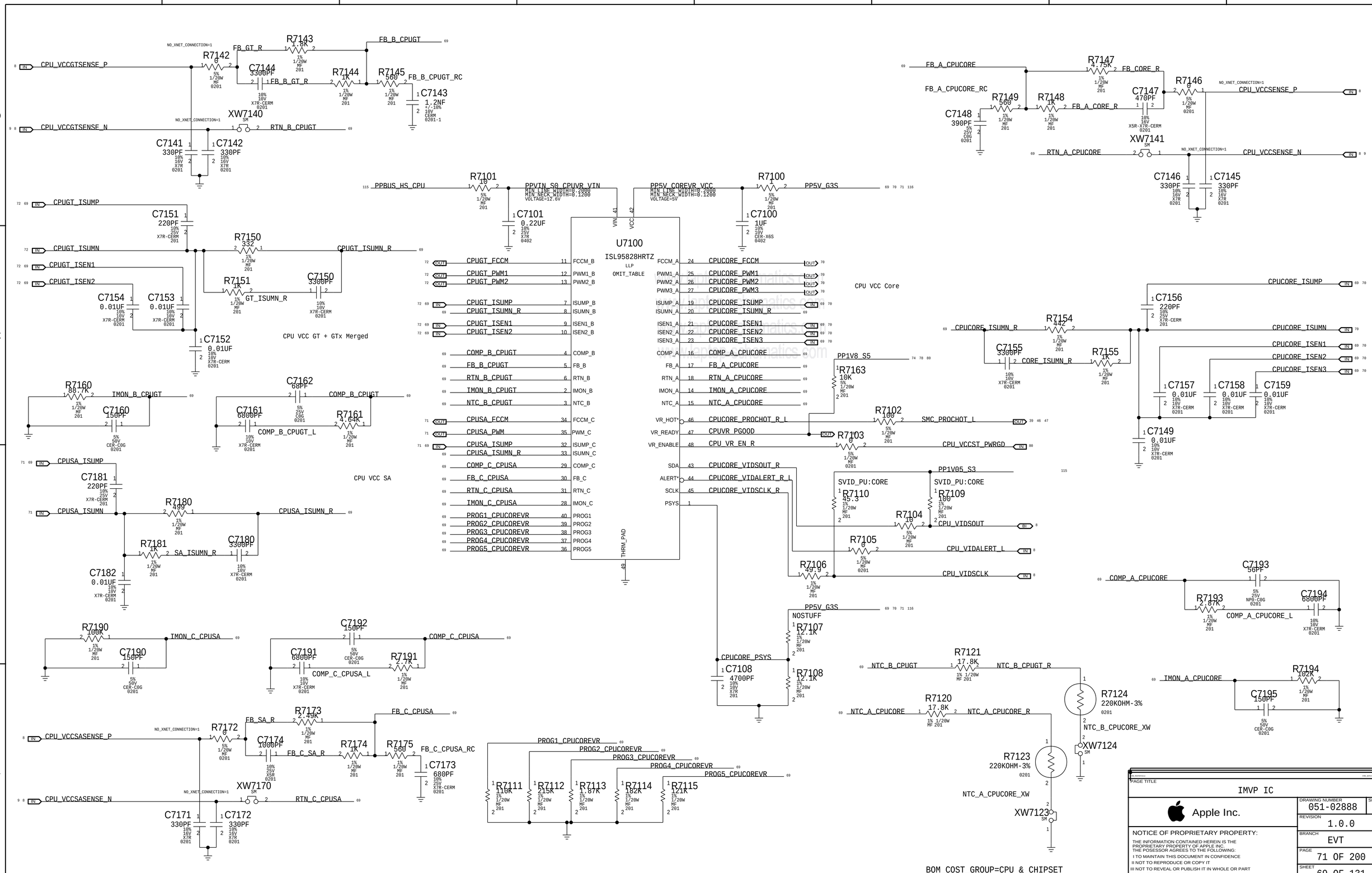


PAGE TITLE

IMVP IC

Apple Inc.

| | |
|---|---|
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
| BRANCH | EVT |
| PAGE | 71 OF 200 |
| SHEET | 69 OF 131 |

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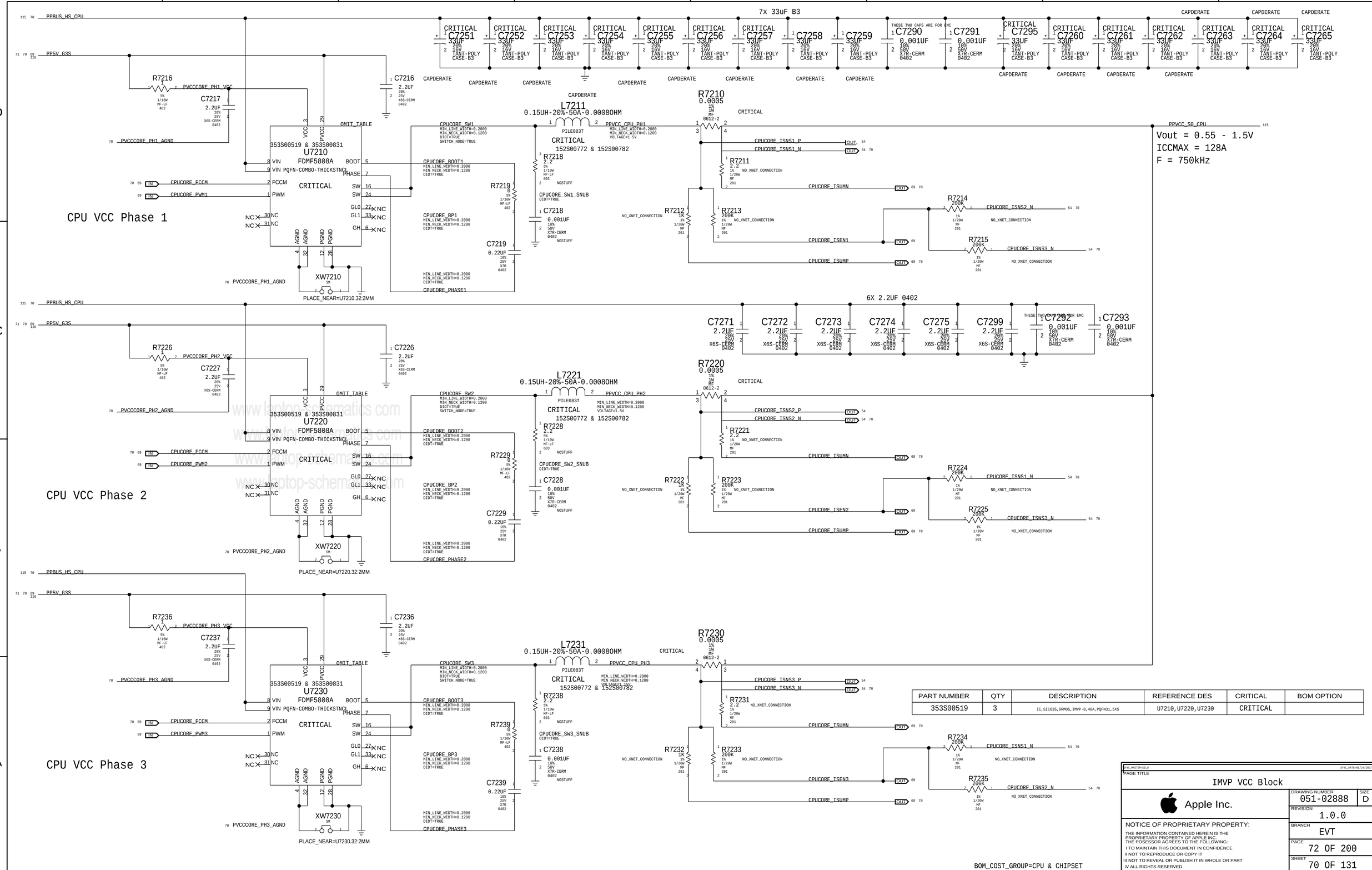


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S00519 | 3 | IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5 | U7210,U7220,U7230 | CRITICAL | |

SYNC_MASTER=J13LU SYNC_DATE=05/24/2017

PAGE TITLE

IMVP VCC Block

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 72 OF 200

SHEET 70 OF 131

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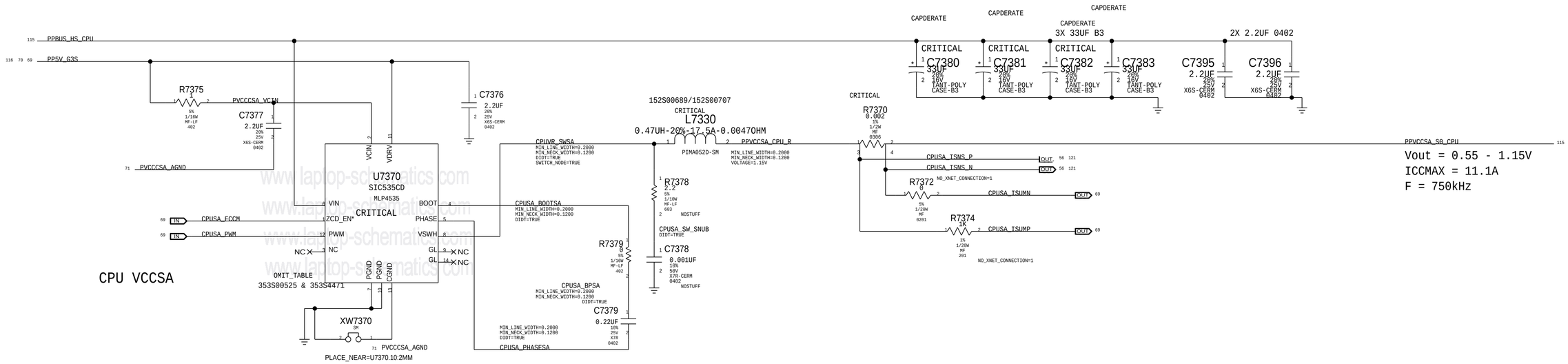


CPU VCCSA

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S00525 | 1 | IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5 | U7370 | CRITICAL | |

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J11J

SYNC_DATE=05/16/2017

PAGE TITLE

IMVP SA Block

Apple Inc.

DRAWING NUMBER 051-02888

SIZE D

REVISION 1.0.0

BRANCH EVT

PAGE 73 OF 200

SHEET 71 OF 131

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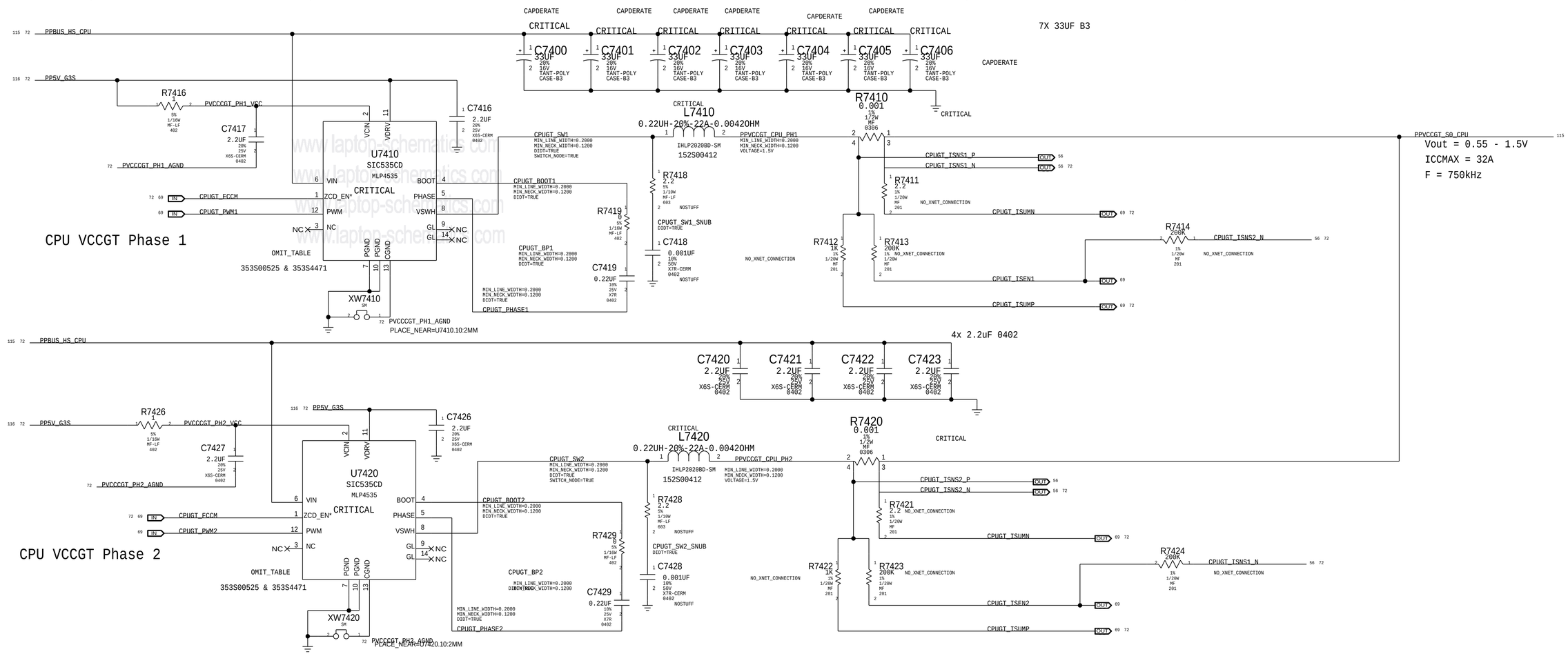


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S00525 | 2 | IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5 | U7410,U7420 | CRITICAL | |

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
IMVP GT Block

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 74 OF 200
SHEET 72 OF 131

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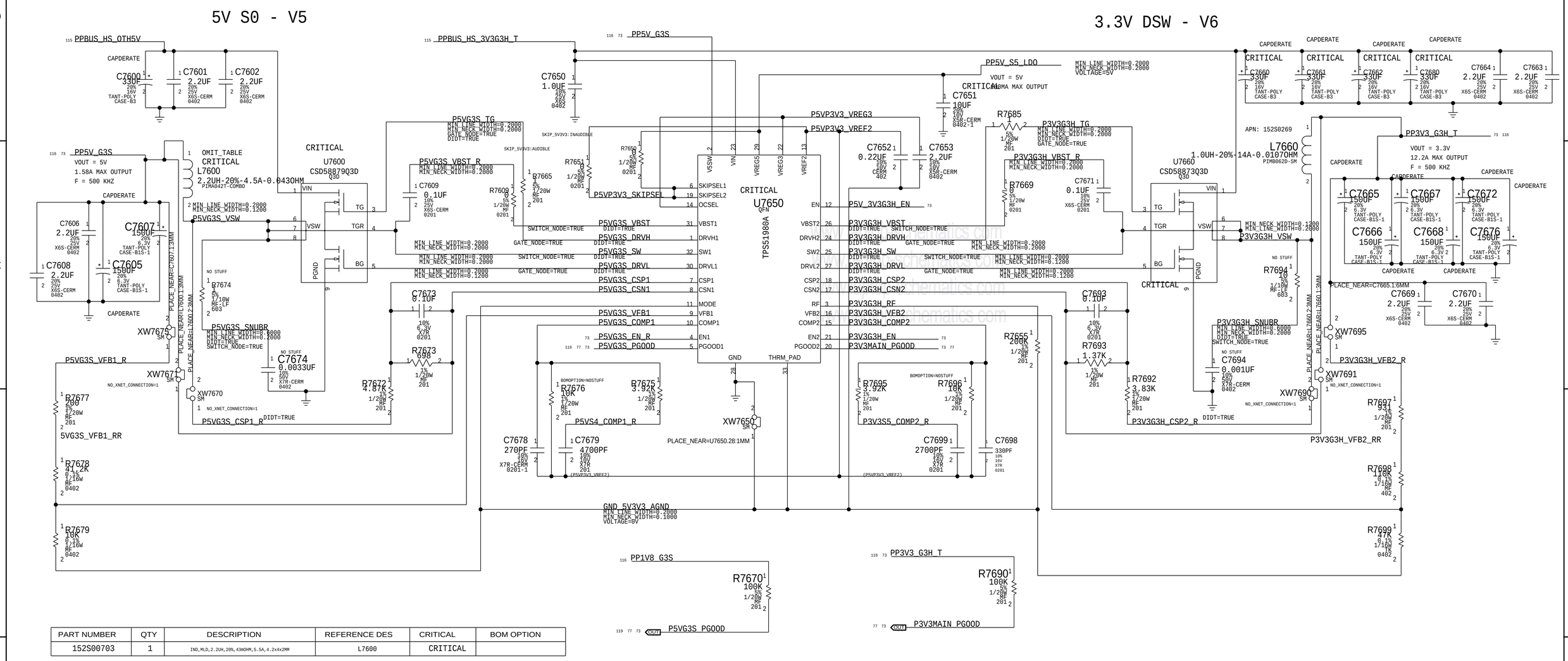
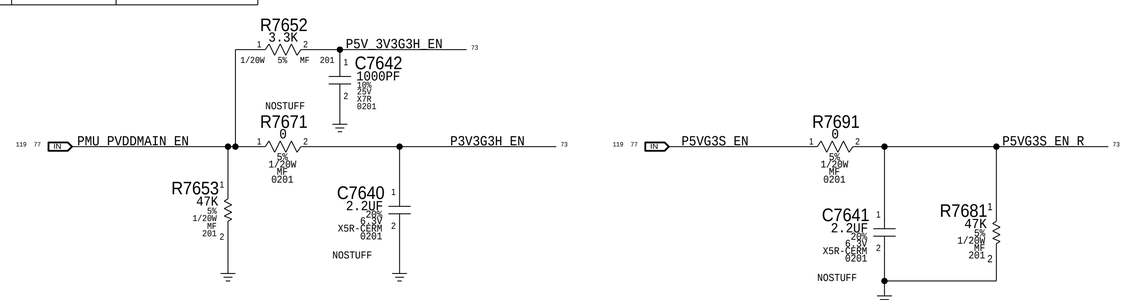



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 152S00703 | 1 | IND,MLD,2.2UH,20%,43mOHM,5.5A,4.2x4x2MM | L7600 | CRITICAL | |




www.schematics.com

PAGE TITLE
Power - 5V 3.3V Supply

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 76 OF 200
SHEET 73 OF 131

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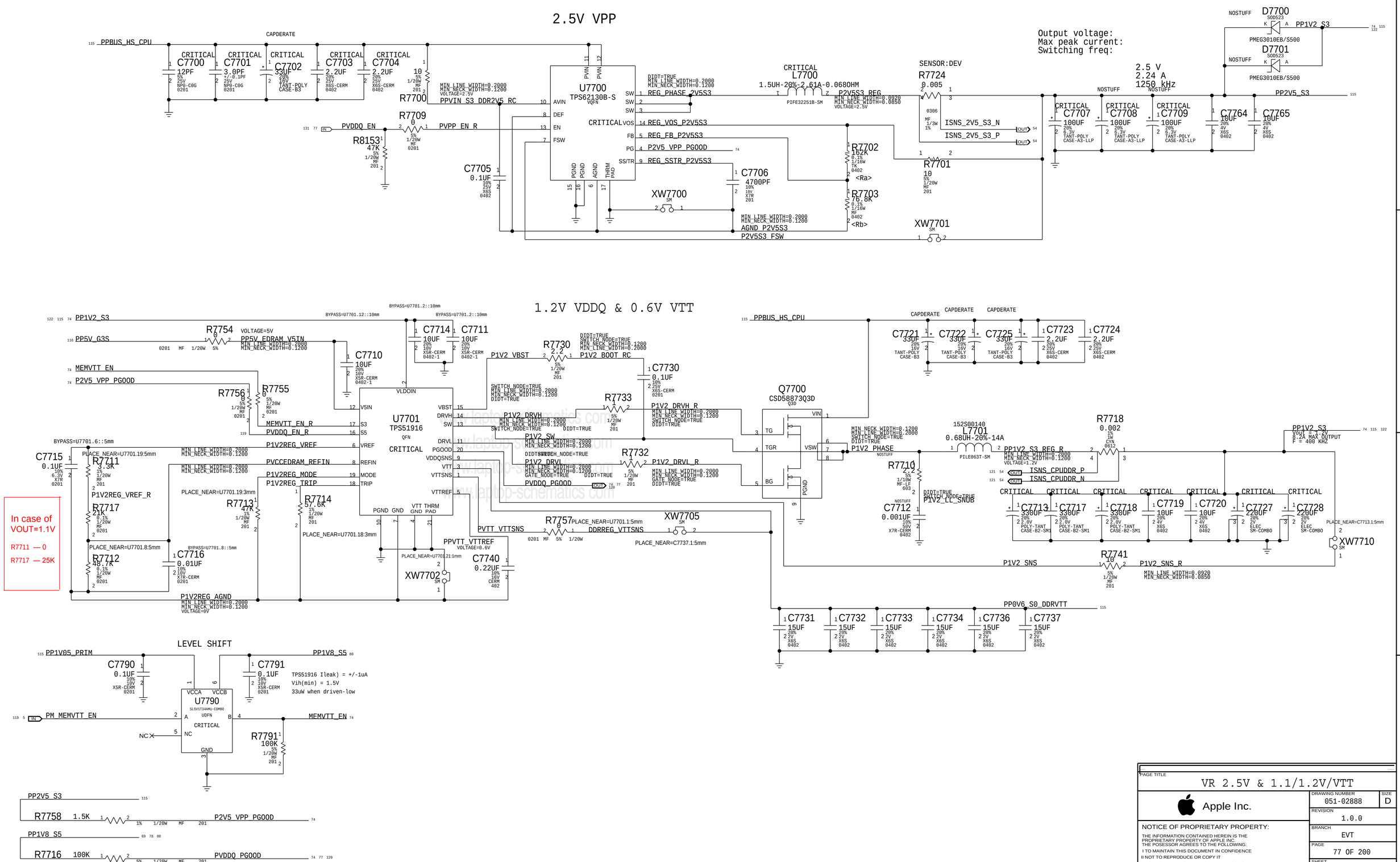


PAGE TITLE: VR 2.5V & 1.1/1.2V/VTT

Apple Inc.

DRAWING NUMBER: 051-02888 | SIZE: D

REVISION: 1.0.0

BRANCH: EVT

PAGE: 77 OF 200

SHEET: 74 OF 131

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Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)

CRITICAL
OMIT_TABLE

U7800
CALPE-PMU
BGA
SYM 2 OF 4
338S00267-A0

PP3V3_G3H_SOCPMU

C7801 10UF 20% 6.3V CER-X6S 0402
C7802 10UF 20% 6.3V CER-X6S 0402
C7803 10UF 20% 6.3V CER-X6S 0402
C7804 10UF 20% 6.3V CER-X6S 0402
C7805 10UF 20% 6.3V CER-X6S 0402
C7810 10UF 20% 6.3V CER-X6S 0402
C7809 10UF 20% 6.3V CER-X6S 0402
C7808 10UF 20% 6.3V CER-X6S 0402
C7807 10UF 20% 6.3V CER-X6S 0402
C7806 10UF 20% 6.3V CER-X6S 0402
C7891 1UF 20% 4V CERM-X6S 0201
C7892 1UF 20% 4V CERM-X6S 0201
C7893 1UF 20% 4V CERM-X6S 0201
C7894 1UF 20% 4V CERM-X6S 0201

PLACE_NEAR=U7800.R1:5MM
PLACE_NEAR=U7800.L1:5MM
PLACE_NEAR=U7800.G1:5MM
PLACE_NEAR=U7800.A7:5MM
PLACE_NEAR=U7800.C1:5MM

C7860 1UF 20% 4V CERM-X6S 0201
C7861 1UF 20% 4V CERM-X6S 0201
C7862 1UF 20% 4V CERM-X6S 0201
C7863 1UF 20% 4V CERM-X6S 0201
C7864 1UF 20% 4V CERM-X6S 0201

PLACE_NEAR=U7800.A11:5MM
PLACE_NEAR=U7800.K18:5MM
PLACE_NEAR=U7800.F18:5MM
PLACE_NEAR=U7800.B18:5MM
PLACE_NEAR=U7800.P18:5MM

C7865 1UF 20% 4V CERM-X6S 0201
C7866 1UF 20% 4V CERM-X6S 0201
C7867 1UF 20% 4V CERM-X6S 0201
C7868 1UF 20% 4V CERM-X6S 0201
C7869 1UF 20% 4V CERM-X6S 0201

Resistor Divider from PBUS
VDD_HI < 3.1V

PMU_VDD_HI

PP1V8_SLPS2R_PMUVDDGPIO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

C7800 0.1UF 10% 6.3V X6S 0201

| Pin | Net |
|---|---|
| P5 | VDD_MAIN_E |
| D10 | VDD_MAIN_N |
| P9 | VDD_MAIN_S |
| K14 | VDD_MAIN_W |
| K13 | VDD_HI |
| J11 | VDD_GPIO |
| C1, C2, C3 | VDD_BUCK0_01 |
| G1, G2, G3 | VDD_BUCK0_23 |
| R1, R2 | VDD_BUCK16 |
| L1, L2, L3 | VDD_BUCK2 |
| B16, B17, B18 | VDD_BUCK3 |
| A7, B7 | VDD_BUCK4 |
| A11, B11 | VDD_BUCK5 |
| F17, F18 | VDD_BUCK7 |
| K16, K17, K18 | VDD_BUCK8 |
| P16, P17, P18 | VDD_BUCK910 |
| NC T1, NC T2 | BUCK6_LX0 |
| R7 | BUCK6_IN |
| NC T4 | BUCK6_FB |
| NC E17, NC E18 | BUCK7_LX0 |
| NC G17, NC G18 | BUCK7_LX1 |
| NC F15 | BUCK7_RTP |
| G15 | BUCK7_RTN |
| L16, L17, L18 | BUCK8_LX0 |
| J16, J17, J18 | BUCK8_LX1 |
| L14 | BUCK8_FB |
| P12, R12, T12, U12, V12 | BUCK8_IN |
| NC N16, NC N17, NC N18 | BUCK9_LX0 |
| NC P14 | BUCK9_RTP |
| N14 | BUCK9_RTN |
| NC R16, NC R17, NC R18 | BUCK10_LX0 |
| NC R14 | BUCK10_FB |

Note : All Bucks are default Local Sense
Buck 0,2, and 8 have option for Remote Sense for Future Use.

PPVDDCPUAWAKE
Vout = 0.625V - 1.06V
Iout_Max = 13.4A
F = 2MHz & 4MHz

BUCK0_LX0 — PVDDCPUAWAKE_SW0 — CRITICAL L7806 1UH-20%-3.8A-0.055OHM 2016-COMBO
BUCK0_LX1 — PVDDCPUAWAKE_SW1 — CRITICAL L7807 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
BUCK0_LX2 — PVDDCPUAWAKE_SW2 — CRITICAL L7808 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
BUCK0_LX3 — PVDDCPUAWAKE_SW3 — CRITICAL L7809 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.6000, DIDT=TRUE

C7821 20UF 20% 2.5V X6S-CERM 0402
C7822 20UF 20% 2.5V X6S-CERM 0402
C7823 20UF 20% 2.5V X6S-CERM 0402
C7824 20UF 20% 2.5V X6S-CERM 0402
C7825 20UF 20% 2.5V X6S-CERM 0402
C7812 20UF 20% 2.5V X6S-CERM 0402
C7811 20UF 20% 2.5V X6S-CERM 0402
C7826 20UF 20% 2.5V X6S-CERM 0402
C7827 20UF 20% 2.5V X6S-CERM 0402
C7828 20UF 20% 2.5V X6S-CERM 0402
C7813 20UF 20% 2.5V X6S-CERM 0402

BUCK0_FB — PVDDCPUAWAKE_FB — R7806 0 0201 1/20W 5% MF — PLACE_NEAR=L7806.2:5MM

PPVDDCPUSRAM_AWAKE
Vout = 0.8V - 1.06V
Iout_Max = 1A
F = 3MHz

BUCK1_LX0 — PVDDCPUSRAMAWAKE_SW0 — CRITICAL L7810 1.0UH-20%-2.6A-0.095OHM 0805-COMBO
BUCK1_FB — PVDDCPUSRAMAWAKE_FB — R7811 0 0201 1/20W 5% MF — PLACE_NEAR=L7810.2:5MM
SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.6000, DIDT=TRUE

C7829 10UF 20% 4V X6S 0402-1
C7830 10UF 20% 4V X6S 0402-1

PP0V82_SLPDDR
Vout = 0.82V
Iout_Max = 6A
F = 3MHz

BUCK2_LX0 — P0V8SLPDDR_SW0 — CRITICAL L7811 1UH-20%-4.7A-0.040HM 2520
BUCK2_LX1 — P0V8SLPDDR_SW1 — CRITICAL L7812 0.47UH-20%-4.8A-0.034OHM 0806
BUCK2_FB — P0V8SLPDDR_FB — R7812 0 0201 1/20W 5% MF — PLACE_NEAR=L7812.2:5MM
SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.6000, DIDT=TRUE

C7833 20UF 20% 2.5V X6S-CERM 0402
C7834 20UF 20% 2.5V X6S-CERM 0402
C7835 20UF 20% 2.5V X6S-CERM 0402
C7836 20UF 20% 2.5V X6S-CERM 0402
C7837 20UF 20% 2.5V X6S-CERM 0402
C7838 20UF 20% 2.5V X6S-CERM 0402
C7814 20UF 20% 2.5V X6S-CERM 0402
C7815 20UF 20% 2.5V X6S-CERM 0402

PP1V8_SLPS2R
Vout = 1.8V
Iout_Max = 2.5A
F = 3MHz

BUCK3_LX0 — P1V8SLPS2R_SW0 — CRITICAL L7813 1UH-20%-3.8A-0.055OHM 2016-COMBO
BUCK3_FB — P1V8SLPS2R_FB — R7813 0 0201 1/20W 5% MF — PLACE_NEAR=L7813.2:5MM
SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.6000, DIDT=TRUE

C7839 20UF 20% 2.5V X6S-CERM 0402
C7840 20UF 20% 2.5V X6S-CERM 0402
C7841 20UF 20% 2.5V X6S-CERM 0402
C7842 20UF 20% 2.5V X6S-CERM 0402
C7843 20UF 20% 2.5V X6S-CERM 0402
C7844 20UF 20% 2.5V X6S-CERM 0402
C7845 20UF 20% 2.5V X6S-CERM 0402

BUCK3_IN — R9, T10, T9, U10, U9, V10, V9 — PP1V8_SLPS2R

PP1V1_SLPS2R
Vout = 1.1V
Iout_Max = 4A
F = 3MHz

BUCK4_LX0 — P1V1SLPS2R_SW0 — CRITICAL L7814 1UH-20%-3.8A-0.055OHM 2016-COMBO
BUCK4_LX1 — P1V1SLPS2R_SW1 — CRITICAL L7815 0.47UH-20%-4.8A-0.034OHM 0806-COMBO
BUCK4_FB — P1V1SLPS2R_FB — R7814 0 0201 1/20W MF 5% — PLACE_NEAR=L7815.2:5MM
SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.6000, DIDT=TRUE
BUCK4_IN — P7

C7846 20UF 20% 2.5V X6S-CERM 0402
C7847 20UF 20% 2.5V X6S-CERM 0402
C7848 20UF 20% 2.5V X6S-CERM 0402
C7849 20UF 20% 2.5V X6S-CERM 0402
C7850 20UF 20% 2.5V X6S-CERM 0402
C7851 20UF 20% 2.5V X6S-CERM 0402
C7816 20UF 20% 2.5V X6S-CERM 0402
C7817 20UF 20% 2.5V X6S-CERM 0402

PP0V9_SLPDDR
Vout = 0.9V
Iout_Max = 4A
F = 3MHz

BUCK5_LX0 — P0V9SLPDDR_SW0 — L7816 2016-COMBO
BUCK5_LX1 — P0V9SLPDDR_SW1 — CRITICAL L7817 0.47UH-20%-4.8A-0.034OHM 0806-COMBO
BUCK5_FB — P0V9SLPDDR_FB — R7816 0 0201 1/20W MF 5% — PLACE_NEAR=L7816.2:5MM
MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, SWITCH_NODE=TRUE, DIDT=TRUE
1UH-20%-3.8A-0.055OHM; 0.47UH-20%-4.8A-0.034OHM

C7852 20UF 20% 2.5V X6S-CERM 0402
C7853 20UF 20% 2.5V X6S-CERM 0402
C7854 20UF 20% 2.5V X6S-CERM 0402
C7855 20UF 20% 2.5V X6S-CERM 0402
C7856 20UF 20% 2.5V X6S-CERM 0402
C7818 20UF 20% 2.5V X6S-CERM 0402
C7819 20UF 20% 2.5V X6S-CERM 0402

PPVCCPRIMCORE_PRIM_REG
Vout = 1.05V
Iout_Max = 6A
F = 3MHz

C7872 20UF 20% 2.5V X6S-CERM 0402
C7873 20UF 20% 2.5V X6S-CERM 0402
C7874 20UF 20% 2.5V X6S-CERM 0402
C7875 20UF 20% 2.5V X6S-CERM 0402
C7876 20UF 20% 2.5V X6S-CERM 0402
C7899 20UF 20% 2.5V X6S-CERM 0402
C7898 20UF 20% 2.5V X6S-CERM 0402
C7877 20UF 20% 2.5V X6S-CERM 0402
C7878 20UF 20% 2.5V X6S-CERM 0402
C7879 20UF 20% 2.5V X6S-CERM 0402
C7880 20UF 20% 2.5V X6S-CERM 0402
C7881 20UF 20% 2.5V X6S-CERM 0402
C7882 20UF 20% 2.5V X6S-CERM 0402
C7883 20UF 20% 2.5V X6S-CERM 0402
C7884 20UF 20% 2.5V X6S-CERM 0402
C7885 20UF 20% 2.5V X6S-CERM 0402
C7886 20UF 20% 2.5V X6S-CERM 0402

CRITICAL L7821 0.47UH-20%-4.8A-0.0340HM 0806-COMBO — PVCCPRIMCORE_SW0
CRITICAL L7822 0.47UH-20%-4.8A-0.0340HM 0806-COMBO — PVCCPRIMCORE_SW1
SWITCH_NODE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, DIDT=TRUE
NOSTUFF R7820 0 0201 5% MF 1/20W — PLACE_NEAR=L7822.1:5MM — PVCCPRIMCORE_FB
R7821 0 0201 5% MF 1/20W — PVCCPRIM_FETIN

| Net | Signal | Supplied Current |
|---|---|---|
| BUCK3_SW1 | PP1V8_AWAKE | 0.3A |
| BUCK3_SW2 | PP1V8_SLPS2R_PMUVDDGPIO | 0.3A |
| BUCK3_SW3 | PP1V8_S5 | 1.0A |
| BUCK3_SW4 | NC_PP1V8_S3 | 1.0A |
| BUCK3_SW5 | NC_PP1V8_S0 | 0.5A |
| BUCK4_SW1 | NC | 0.5A |
| BUCK6_SW1 | NC | 0.3A |
| BUCK8_SW1 | NC | 0.3A |
| BUCK8_SW2 | PP1V05_S3 | 0.3A |

BOM_COST_GROUP=SOC

PAGE TITLE: PMIC BUCKS AND SWs

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DRAWING NUMBER: 051-02888 SIZE: D
REVISION: 1.0.0
BRANCH: EVT
PAGE: 78 OF 200
SHEET: 75 OF 131

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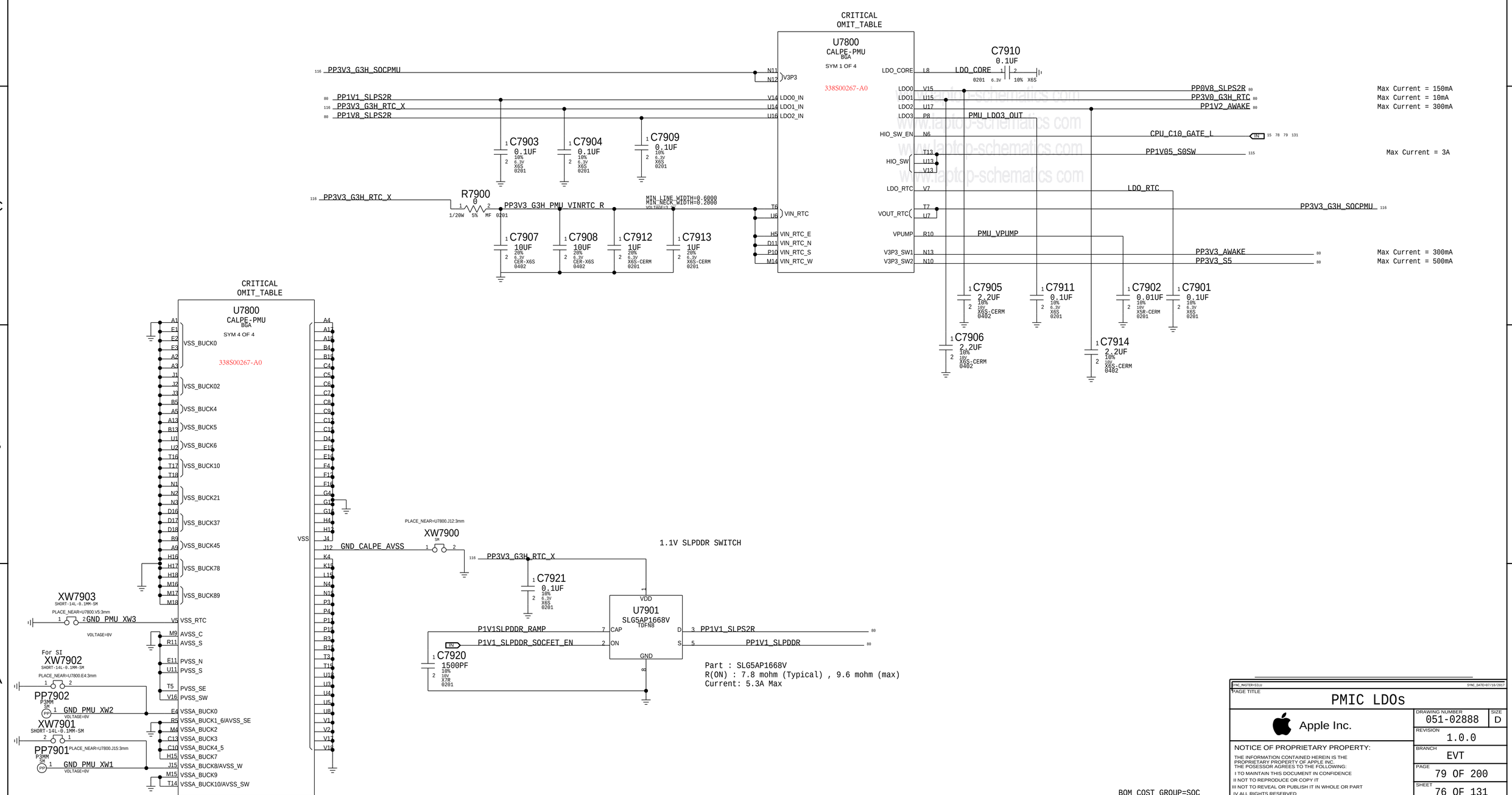
CRITICAL
OMIT_TABLE
U7800
CALPE-PMU
BGA
SYM 1 OF 4
338S00267-A0
PP3V3_G3H_SOCPMU
PP1V1_SLPS2R
PP3V3_G3H_RTC_X
PP1V8_SLPS2R
V3P3
LDO0_IN
LDO1_IN
LDO2_IN
C7903 0.1UF 10% 6.3V X6S 0201
C7904 0.1UF 10% 6.3V X6S 0201
C7909 0.1UF 10% 6.3V X6S 0201
R7900 0 1/20W 5% MF 0201
PP3V3_G3H_PMU_VINRTC_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3
C7907 10UF 20% 6.3V CER-X6S 0402
C7908 10UF 20% 6.3V CER-X6S 0402
C7912 1UF 20% 6.3V X6S-CERM 0201
C7913 1UF 20% 6.3V X6S-CERM 0201
VIN_RTC
VIN_RTC_E
VIN_RTC_N
VIN_RTC_S
VIN_RTC_W
LDO_CORE
C7910 0.1UF 0201 6.3V 10% X6S
LDO0
LDO1
LDO2
LDO3
PP0V8_SLPS2R
PP3V0_G3H_RTC
PP1V2_AWAKE
Max Current = 150mA
Max Current = 10mA
Max Current = 300mA
PMU_LDO3_OUT
HIO_SW_EN
CPU_C10_GATE_L
HIO_SW
PP1V05_S0SW
Max Current = 3A
LDO_RTC
VOUT_RTC
PP3V3_G3H_SOCPMU
VPUMP
PMU_VPUMP
V3P3_SW1
V3P3_SW2
PP3V3_AWAKE
PP3V3_S5
Max Current = 300mA
Max Current = 500mA
C7905 2.2UF 10% 10V X6S-CERM 0402
C7906 2.2UF 10% 10V X6S-CERM 0402
C7911 0.1UF 10% 6.3V X6S 0201
C7914 2.2UF 10% 10V X6S-CERM 0402
C7902 0.01UF 10% 10V X5R-CERM 0201
C7901 0.1UF 10% 6.3V X6S 0201
CRITICAL
OMIT_TABLE
U7800
CALPE-PMU
BGA
SYM 4 OF 4
338S00267-A0
VSS_BUCK0
VSS_BUCK02
VSS_BUCK4
VSS_BUCK5
VSS_BUCK6
VSS_BUCK10
VSS_BUCK21
VSS_BUCK37
VSS_BUCK45
VSS_BUCK78
VSS_BUCK89
VSS_RTC
AVSS_C
AVSS_S
PVSS_N
PVSS_S
PVSS_SE
PVSS_SW
VSSA_BUCK0
VSSA_BUCK1_6/AVSS_SE
VSSA_BUCK2
VSSA_BUCK3
VSSA_BUCK4_5
VSSA_BUCK7
VSSA_BUCK8/AVSS_W
VSSA_BUCK9
VSSA_BUCK10/AVSS_SW
VSS
GND_CALPE_AVSS
PLACE_NEAR=U7800.J12:3mm
XW7900
SM
PP3V3_G3H_RTC_X
C7921 0.1UF 10% 6.3V X6S 0201
1.1V SLPDDR SWITCH
U7901
SLG5AP1668V
TDFN8
VDD
CAP
ON
GND
D
S
PP1V1_SLPS2R
PP1V1_SLPDDR
P1V1SLPDDR_RAMP
P1V1_SLPDDR_SOCFET_EN
C7920 1500PF 10% 10V X7R 0201
Part : SLG5AP1668V
R(ON) : 7.8 mohm (Typical) , 9.6 mohm (max)
Current: 5.3A Max
XW7903
SHORT-14L-0.1MM-SM
PLACE_NEAR=U7800.V5:3mm
GND_PMU_XW3
VOLTAGE=0V
For SI
XW7902
SHORT-14L-0.1MM-SM
PLACE_NEAR=U7800.E4:3mm
PP7902
P3MM
SM
GND_PMU_XW2
XW7901
SHORT-14L-0.1MM-SM
PP7901
PLACE_NEAR=U7800.J15:3mm
GND_PMU_XW1
BOM_COST_GROUP=SOC
SYNC_MASTER=SELU
SYNC_DATE=07/10/2017
PAGE TITLE
PMIC LDOs
Apple Inc.
DRAWING NUMBER
051-02888
SIZE
D
REVISION
1.0.0
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PAGE
79 OF 200
SHEET
76 OF 131
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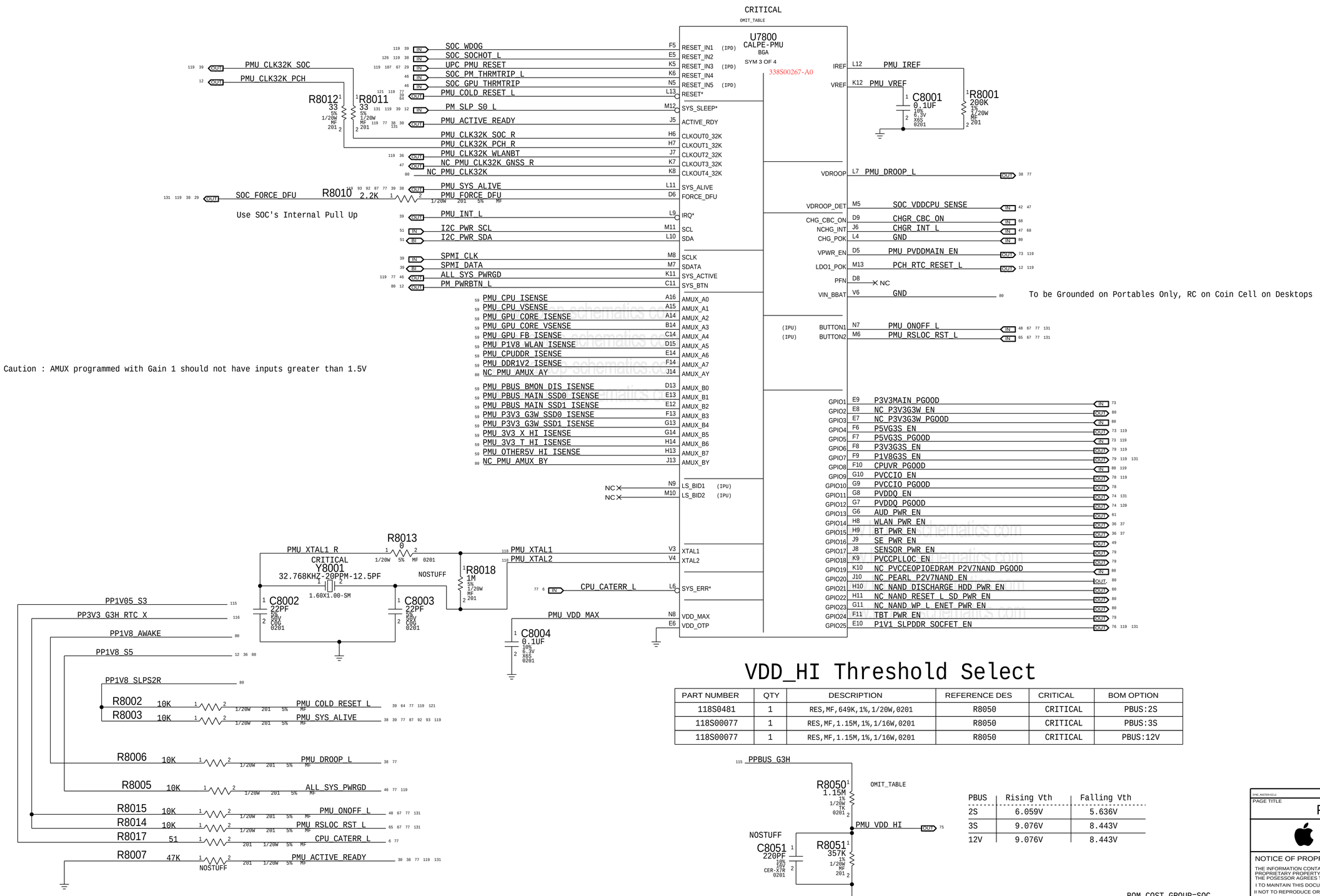


# VDD_HI Threshold Select

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 118S0481 | 1 | RES,MF,649K,1%,1/20W,0201 | R8050 | CRITICAL | PBUS:2S |
| 118S00077 | 1 | RES,MF,1.15M,1%,1/16W,0201 | R8050 | CRITICAL | PBUS:3S |
| 118S00077 | 1 | RES,MF,1.15M,1%,1/16W,0201 | R8050 | CRITICAL | PBUS:12V |

| PBUS | Rising Vth | Falling Vth |
|---|---|---|
| 2S | 6.059V | 5.636V |
| 3S | 9.076V | 8.443V |
| 12V | 9.076V | 8.443V |

PAGE TITLE
PMIC GPIOs & Control

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REVISION 1.0.0
BRANCH EVT
PAGE 80 OF 200
SHEET 77 OF 131

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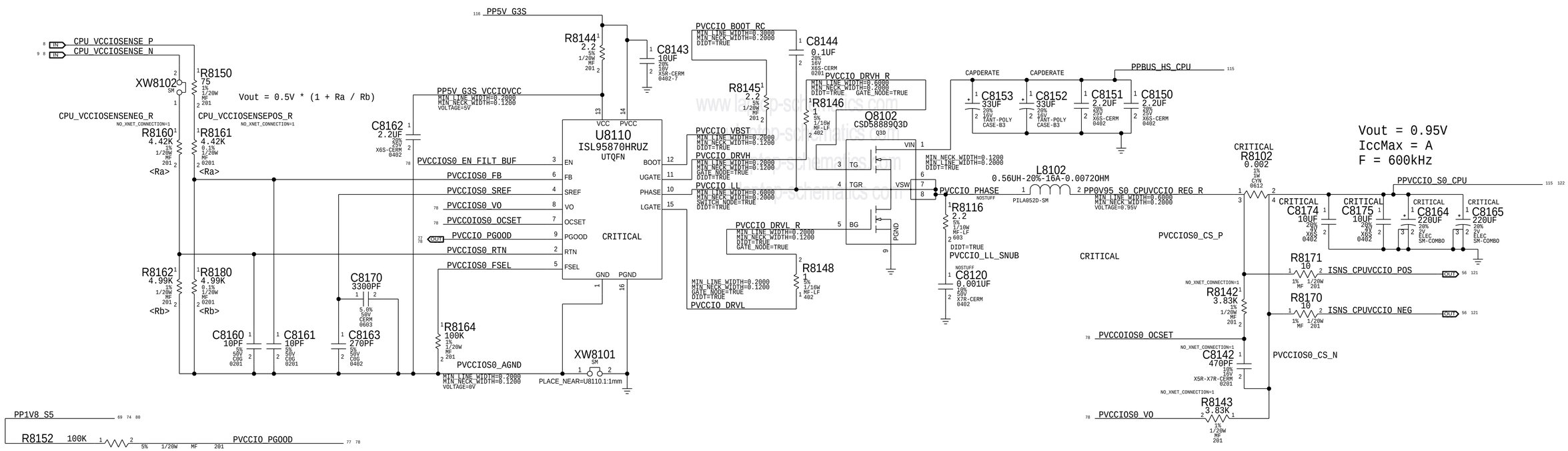
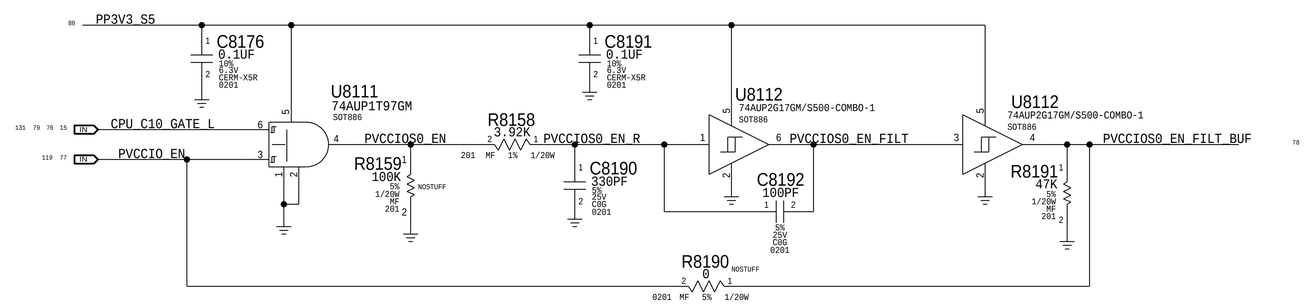
# 0.95V VCCIO




# VCCIO ENABLE LOGIC




BOM_COST_GROUP=PLATFORM POWER

| | |
|---|---|
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| | BRANCH EVT |
| | PAGE 81 OF 200 |
| | SHEET 78 OF 131 |

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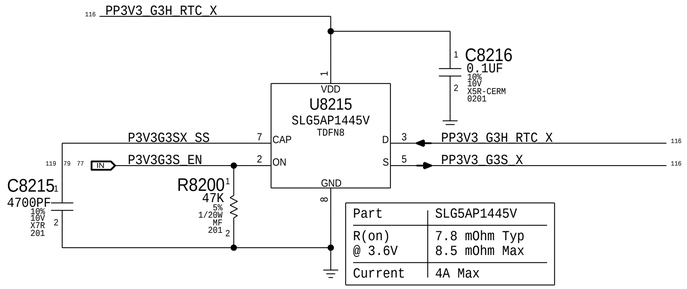
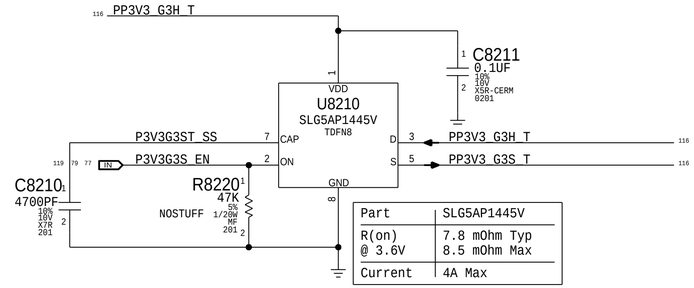
## 3.3V G3 Standby Switch X



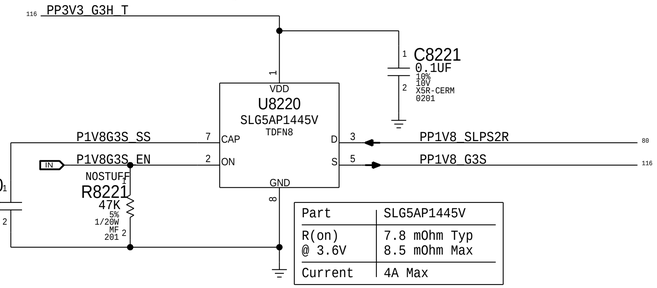

| Part | SLG5AP1445V |
|---|---|
| R(on) @ 3.6V | 7.8 mOhm Typ<br>8.5 mOhm Max |
| Current | 4A Max |

## 3.3V G3 Standby Switch T



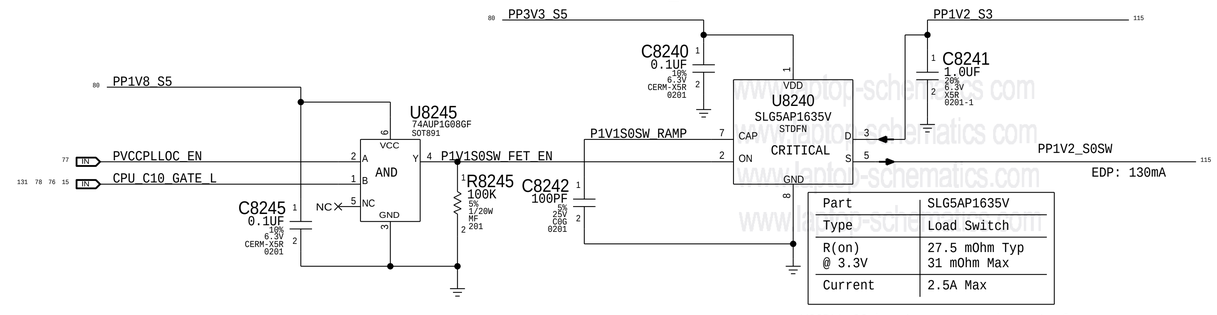

| Part | SLG5AP1445V |
|---|---|
| R(on) @ 3.6V | 7.8 mOhm Typ<br>8.5 mOhm Max |
| Current | 4A Max |

## 1.8V G3 Standby Switch




| Part | SLG5AP1445V |
|---|---|
| R(on) @ 3.6V | 7.8 mOhm Typ<br>8.5 mOhm Max |
| Current | 4A Max |

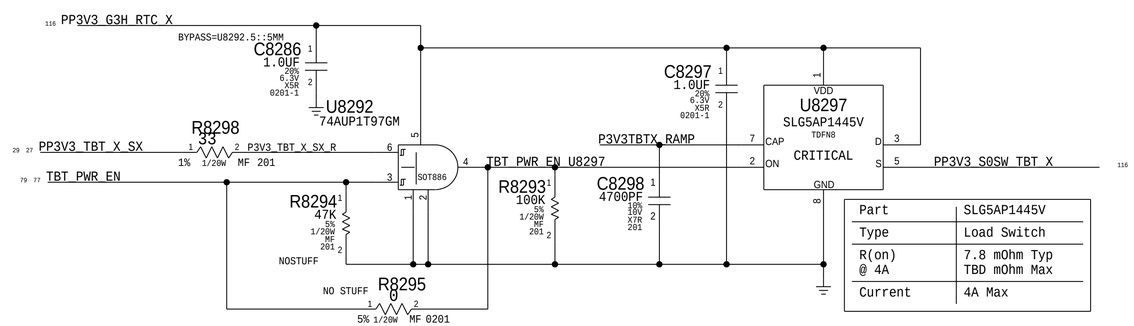
## 1.1V S0SW VCCPLL_OC Switch




| Part | SLG5AP1635V |
|---|---|
| Type | Load Switch |
| R(on) @ 3.3V | 27.5 mOhm Typ<br>31 mOhm Max |
| Current | 2.5A Max |

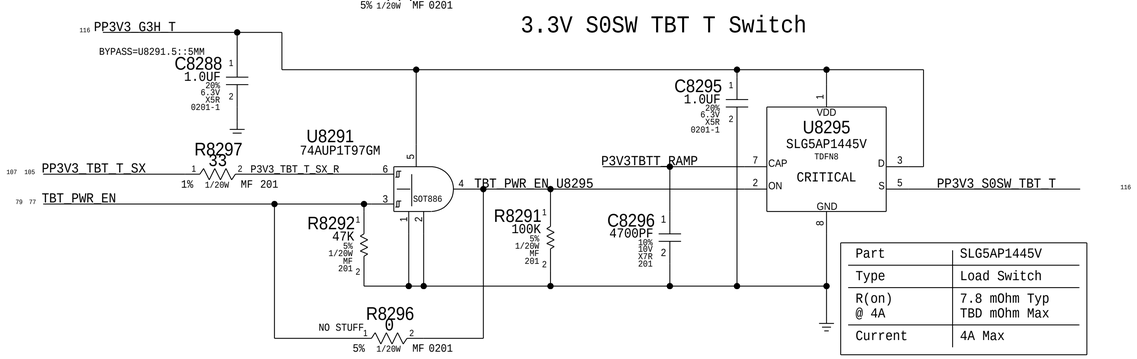
VCCPLL_OC has turn-on requirement of
11uS min and 240uS max
from EN to 1.1V

## 3.3V S0SW TBT X Switch



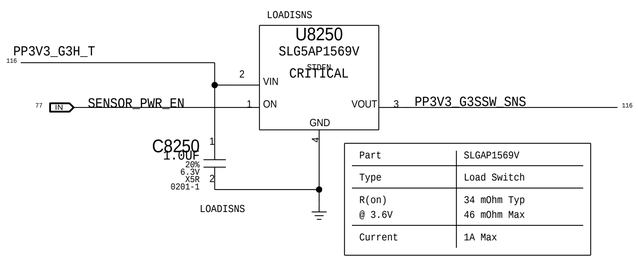

| Part | SLG5AP1445V |
|---|---|
| Type | Load Switch |
| R(on) @ 4A | 7.8 mOhm Typ<br>TBD mOhm Max |
| Current | 4A Max |

## 3.3V S0SW TBT T Switch




| Part | SLG5AP1445V |
|---|---|
| Type | Load Switch |
| R(on) @ 4A | 7.8 mOhm Typ<br>TBD mOhm Max |
| Current | 4A Max |

## 3.3V Sensor Switch




| Part | SLGAP1569V |
|---|---|
| Type | Load Switch |
| R(on) @ 3.6V | 34 mOhm Typ<br>46 mOhm Max |
| Current | 1A Max |

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=SILU

PAGE TITLE: Power FETs

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| | |
|---|---|
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
| BRANCH | EVT |
| PAGE | 82 OF 200 |
| SHEET | 79 OF 131 |

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## PMIC Buck0 - SoC VDD_CPU

```
122 75 PPVDDCPU_AWAKE
       PPVDDCPU_AWAKE  MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.05V MAKE_BASE=TRUE  119
       PPVDDCPU_AWAKE  42 80
```

## PMIC Buck1 - SoC VDD_CPU_SRAM

```
122 75 PPVDDCPUSRAM_AWAKE
       PPVDDCPUSRAM_AWAKE  MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.05V MAKE_BASE=TRUE  119
       PPVDDCPUSRAM_AWAKE  42
```

## PMIC Buck2 - SoC VDD_SOC

```
75 PP0V82_SLPDDR
   PP0V82_SLPDDR  MIN_LINE_WIDTH=0.7000 MIN_NECK_WIDTH=0.1200 VOLTAGE=0.82V MAKE_BASE=TRUE  119
   PP0V82_SLPDDR  42 80
```

## PMIC BUCK3 - SoC AOP/SMC/VDD1

```
131 122 75 PP1V8_SLPS2R
           PP1V8_SLPS2R  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V MAKE_BASE=TRUE  119
           PP1V8_SLPS2R  75
           PP1V8_SLPS2R  79
           PP1V8_SLPS2R  76
           PP1V8_SLPS2R  46
           PP1V8_SLPS2R  77
           PP1V8_SLPS2R  64
           PP1V8_SLPS2R  46
           PP1V8_SLPS2R  38 47
           PP1V8_SLPS2R  44
           PP1V8_SLPS2R  44
           PP1V8_SLPS2R  44
           PP1V8_SLPS2R  44
           PP1V8_SLPS2R  68
           PP1V8_SLPS2R  51
           PP1V8_SLPS2R  51
           PP1V8_SLPS2R  51
           PP1V8_SLPS2R  47
           PP1V8_SLPS2R  29 107
           PP1V8_SLPS2R  67
           PP1V8_SLPS2R  126 131
           PP1V8_SLPS2R  107
```

## PMIC BUCK3 SW 1

```
131 75 PP1V8_AWAKE
       PP1V8_AWAKE  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V MAKE_BASE=TRUE  119
       PP1V8_AWAKE  77
       PP1V8_AWAKE  46
       PP1V8_AWAKE  44
       PP1V8_AWAKE  44
       PP1V8_AWAKE  44
       PP1V8_AWAKE  44
       PP1V8_AWAKE  44
       PP1V8_AWAKE  41 46 47
       PP1V8_AWAKE  46
       PP1V8_AWAKE  66
       PP1V8_AWAKE  126
```

## PMIC BUCK3 SW 3

```
75 PP1V8_S5
   PP1V8_S5  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V MAKE_BASE=TRUE  119
   PP1V8_S5  46
   PP1V8_S5  16 17
   PP1V8_S5  39
   PP1V8_S5  12 16
   PP1V8_S5  12 13 15 16 19 20 52
   PP1V8_S5  15
   PP1V8_S5  126
   PP1V8_S5  17
   PP1V8_S5
   PP1V8_S5  12 36 77
   PP1V8_S5  51
   PP1V8_S5  51
   PP1V8_S5  51
   PP1V8_S5  46
   PP1V8_S5  94
   PP1V8_S5
   PP1V8_S5  69 74 78
   PP1V8_S5  93
   PP1V8_S5  79
   PP1V8_S5  74
   PP1V8_S5  16
   PP1V8_S5  57
   PP1V8_S5  57
   PP1V8_S5  57
   PP1V8_S5  46
   PP1V8_S5  18
```

## PMIC BUCK3 SW 4/5

```
75 NC_PP1V8_S3
   NC_PP1V8_S3  MAKE_BASE=TRUE  NO_TEST=1
75 NC_PP1V8_S0
   NC_PP1V8_S0  MAKE_BASE=TRUE  NO_TEST=1
```

## PMIC Buck4 - SDRAM VDD2

```
122 75 PP1V1_SLPS2R
       PP1V1_SLPS2R  MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.1V MAKE_BASE=TRUE  119
       PP1V1_SLPS2R  76
       PP1V1_SLPS2R  76
       PP1V1_SLPS2R  43
       PP1V1_SLPS2R  44
```

## Buck 4 Ext. SW U7901 - VDDIO_DDR & PLL

```
76 PP1V1_SLPDDR
   PP1V1_SLPDDR  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.1V MAKE_BASE=TRUE  119
   PP1V1_SLPDDR  38
   PP1V1_SLPDDR  43
   PP1V1_SLPDDR  43
   PP1V1_SLPDDR  44
```

## PMIC Buck5 - VDD_FIXED

```
122 75 PP0V9_SLPDDR
       PP0V9_SLPDDR  MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1200 VOLTAGE=0.9V MAKE_BASE=TRUE  119
       PP0V9_SLPDDR  43
       PP0V9_SLPDDR  43
       PP0V9_SLPDDR  43
       PP0V9_SLPDDR  43
       PP0V9_SLPDDR  43
```

## PMIC LDO0 - VDD_LOW

```
76 PP0V8_SLPS2R
   PP0V8_SLPS2R  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=0.8V MAKE_BASE=TRUE  119
   PP0V8_SLPS2R  43
```

## PMIC LDO2 - PCIE_REFBUF/PLL

```
76 PP1V2_AWAKE
   PP1V2_AWAKE  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.2V MAKE_BASE=TRUE  119
   PP1V2_AWAKE  44
   PP1V2_AWAKE  44
   PP1V2_AWAKE  44
   PP1V2_AWAKE  44
```

## PMIC V3P3 SW 1 - USB

```
76 PP3V3_AWAKE
   PP3V3_AWAKE  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_AWAKE  44
```

## PMIC V3P3 SW 2 (Internal) -

```
76 PP3V3_S5
   PP3V3_S5  MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1750 VOLTAGE=3.3V MAKE_BASE=TRUE  119
   PP3V3_S5  12 16 17
   PP3V3_S5  46
   PP3V3_S5  78
   PP3V3_S5  15 16 19
   PP3V3_S5  14 16
   PP3V3_S5  15 16
   PP3V3_S5  18
   PP3V3_S5  20
   PP3V3_S5  12 16 17
   PP3V3_S5  79
   PP3V3_S5  12
   PP3V3_S5  93 124
   PP3V3_S5  126 131
   PP3V3_S5  16
   PP3V3_S5
```

## PMIC LDO 1 - PCH VCCRTC

```
76 PP3V0_G3H_RTC
   PP3V0_G3H_RTC  MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.0V MAKE_BASE=TRUE  119
   PP3V0_G3H_RTC  12 16 17
```

## NC Aliases

```
77 NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD  MAKE_BASE  NO_TEST  NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD
77 NC_PEARL_P2V7NAND_EN              MAKE_BASE  NO_TEST  NC_PEARL_P2V7NAND_EN
77 NC_NAND_DISCHARGE_HDD_PWR_EN      MAKE_BASE  NO_TEST  NC_NAND_DISCHARGE_HDD_PWR_EN
77 NC_NAND_RESET_L_SD_PWR_EN         MAKE_BASE  NO_TEST  NC_NAND_RESET_L_SD_PWR_EN
77 NC_NAND_WP_L_ENET_PWR_EN          MAKE_BASE  NO_TEST  NC_NAND_WP_L_ENET_PWR_EN
77 NC_P3V3G3W_PGOOD                  MAKE_BASE  NO_TEST  NC_P3V3G3W_PGOOD
77 NC_P3V3G3W_EN                     MAKE_BASE  NO_TEST  NC_P3V3G3W_EN
```

## Alternate Feedback Sesne

```
NOSTUFF
R8320 0 5% 1/16W MF-LF 402  PLACE_NEAR=R7806.1:5MM
XW8320 SM  PLACE_NEAR=U3900.AA12:4MM
75 OUT PVDDCPUAWAKE_FB  Buck0 - Remote  1 R8320 2  PVDDCPUAWAKE_FB_R  1 XW8320 2  PPVDDCPU_AWAKE  42 80

NOSTUFF
R8321 0 5% 1/16W MF-LF 402  PLACE_NEAR=R7812.1:5MM
XW8321 SM  PLACE_NEAR=U3900.AA20:6MM
75 OUT P0V8SLPDDR_FB  Buck2 - Remote  1 R8321 2  P0V8SLPDDR_FB_R  1 XW8321 2  PP0V82_SLPDDR  42 80

R8322 0 5% 1/16W MF-LF 402  PLACE_NEAR=R7820.2:5MM
XW8322 SM  PLACE_NEAR=U1200.AB12:4MM
75 OUT PVCCPRIMCORE_FB  Buck8 - Remote  1 R8322 2  PVCCPRIMCORE_FB_R  1 XW8322 2  PP1V05_PRIM  16 17 115
```

```
NC_CHGR_AUX_OK   NO_TEST=1 MAKE_BASE  NC_CHGR_AUX_OK   68
119 18 PM_PWRBTN_L   MAKE_BASE  PM_PWRBTN_L   12 77
119 77 CPUVR_PGOOD   MAKE_BASE  CPUVR_PGOOD   69
46 8 CPU_VCCST_PWRGD   MAKE_BASE  CPU_VCCST_PWRGD   69
NC_PMU_CLK32K   NO_TEST=1 MAKE_BASE  NC_PMU_CLK32K   77
NC_PMU_AMUX_BY  NO_TEST=1 MAKE_BASE  NC_PMU_AMUX_BY  77
NC_PMU_AMUX_AY  NO_TEST=1 MAKE_BASE  NC_PMU_AMUX_AY  77
```

```
77 GND  MAKE_BASE
77 GND  MAKE_BASE
```

PAGE TITLE

# SOC/PMIC Aliases

Apple Inc.

| | |
|---|---|
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
| BRANCH | EVT |
| PAGE | 83 OF 200 |
| SHEET | 80 OF 131 |

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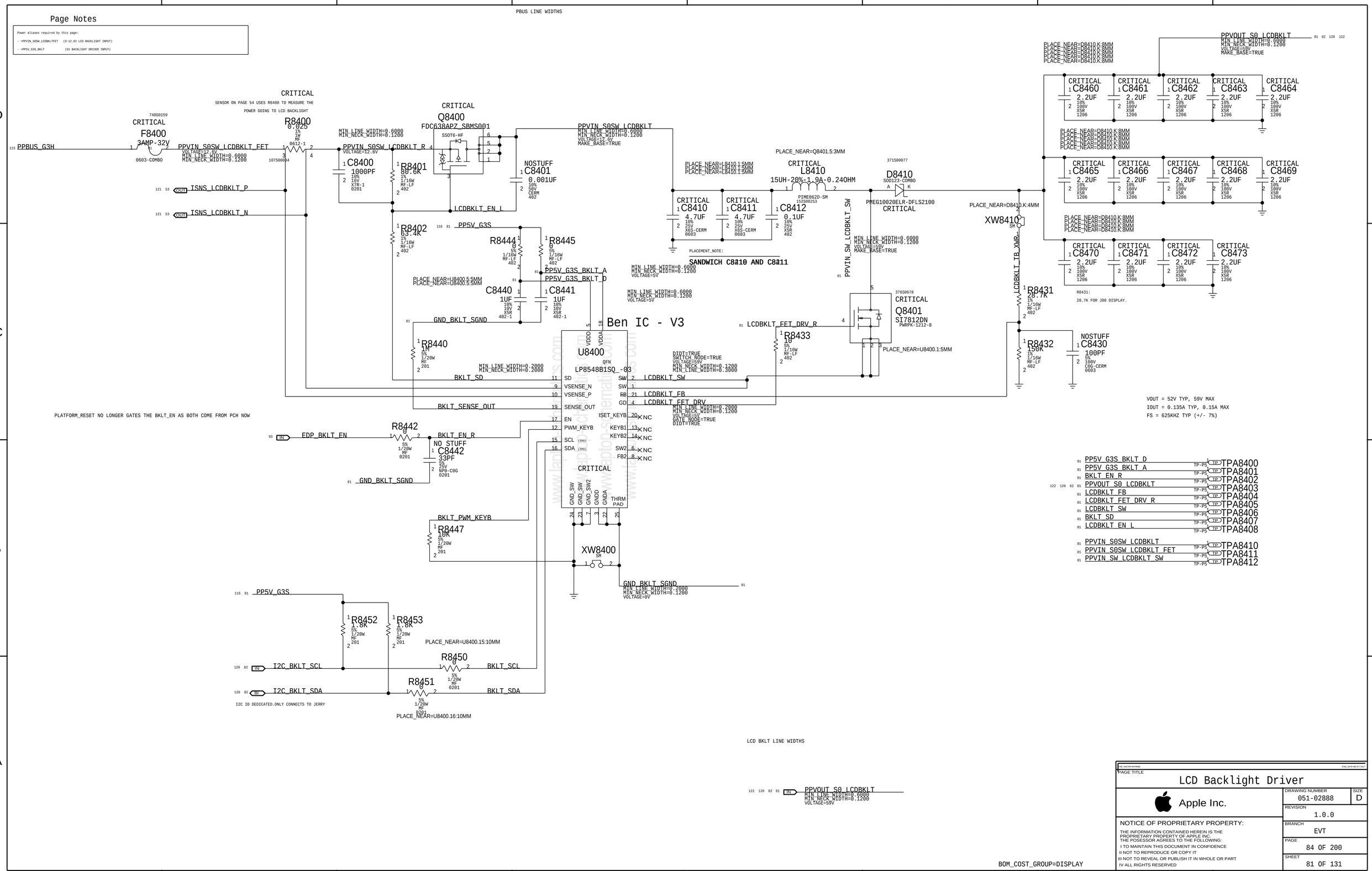
Page Notes
Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (8-12.6V LCD BACKLIGHT INPUT)
- =PP5V_G3S_BKLT (5V BACKLIGHT DRIVER INPUT)
PBUS LINE WIDTHS
PPBUS_G3H
F8400 3AMP-32V
PPVIN_S0SW_LCDBKLT_FET
R8400 0.025
SENSOR ON PAGE 54 USES R8400 TO MEASURE THE POWER GOING TO LCD BACKLIGHT
Q8400 FDC638APZ_SBMS001
PPVIN_S0SW_LCDBKLT_R
C8400 1000PF
R8401 80.6K
NOSTUFF C8401 0.001UF
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
R8402 93.4K
PP5V_G3S
R8444 0
R8445 0
PP5V_G3S_BKLT_A
PP5V_G3S_BKLT_D
C8440 1UF
C8441 1UF
GND_BKLT_SGND
R8440 1M
Ben IC - V3
U8400 LP8548B1SQ_-03
BKLT_SD
BKLT_SENSE_OUT
PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW
EDP_BKLT_EN
R8442 0
BKLT_EN_R
NO STUFF C8442 33PF
GND_BKLT_SGND
BKLT_PWM_KEYB
R8447 10K
XW8400
GND_BKLT_SGND
PPVIN_S0SW_LCDBKLT
PPVIN_S0SW_LCDBKLT_FET
PPVIN_SW_LCDBKLT_SW
L8410 15UH-20%-1.9A-0.240HM
D8410 SDD123-COMBO
PMEG10020ELR-DFLS2100
C8410 4.7UF
C8411 4.7UF
C8412 0.1UF
SANDWICH C8410 AND C8411
Q8401 SI7812DN
R8433 10
LCDBKLT_FET_DRV_R
XW8410
LCDBKLT_TB_XWR
R8431 28.7K
R8432 150K
NOSTUFF C8430 100PF
R8431: 28.7K FOR J80 DISPLAY.
PPVOUT_S0_LCDBKLT
C8460 2.2UF
C8461 2.2UF
C8462 2.2UF
C8463 2.2UF
C8464 2.2UF
C8465 2.2UF
C8466 2.2UF
C8467 2.2UF
C8468 2.2UF
C8469 2.2UF
C8470 2.2UF
C8471 2.2UF
C8472 2.2UF
C8473 2.2UF
VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)
PP5V_G3S
R8452 1.8K
R8453 1.8K
PLACE_NEAR=U8400.15:10MM
I2C_BKLT_SCL
I2C_BKLT_SDA
R8450 0
R8451 0
BKLT_SCL
BKLT_SDA
I2C ID DEDICATED.ONLY CONNECTS TO JERRY
PLACE_NEAR=U8400.16:10MM
TPA8400
TPA8401
TPA8402
TPA8403
TPA8404
TPA8405
TPA8406
TPA8407
TPA8408
TPA8410
TPA8411
TPA8412
LCD BKLT LINE WIDTHS
PPVOUT_S0_LCDBKLT
BOM_COST_GROUP=DISPLAY
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
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PAGE 84 OF 200
SHEET 81 OF 131
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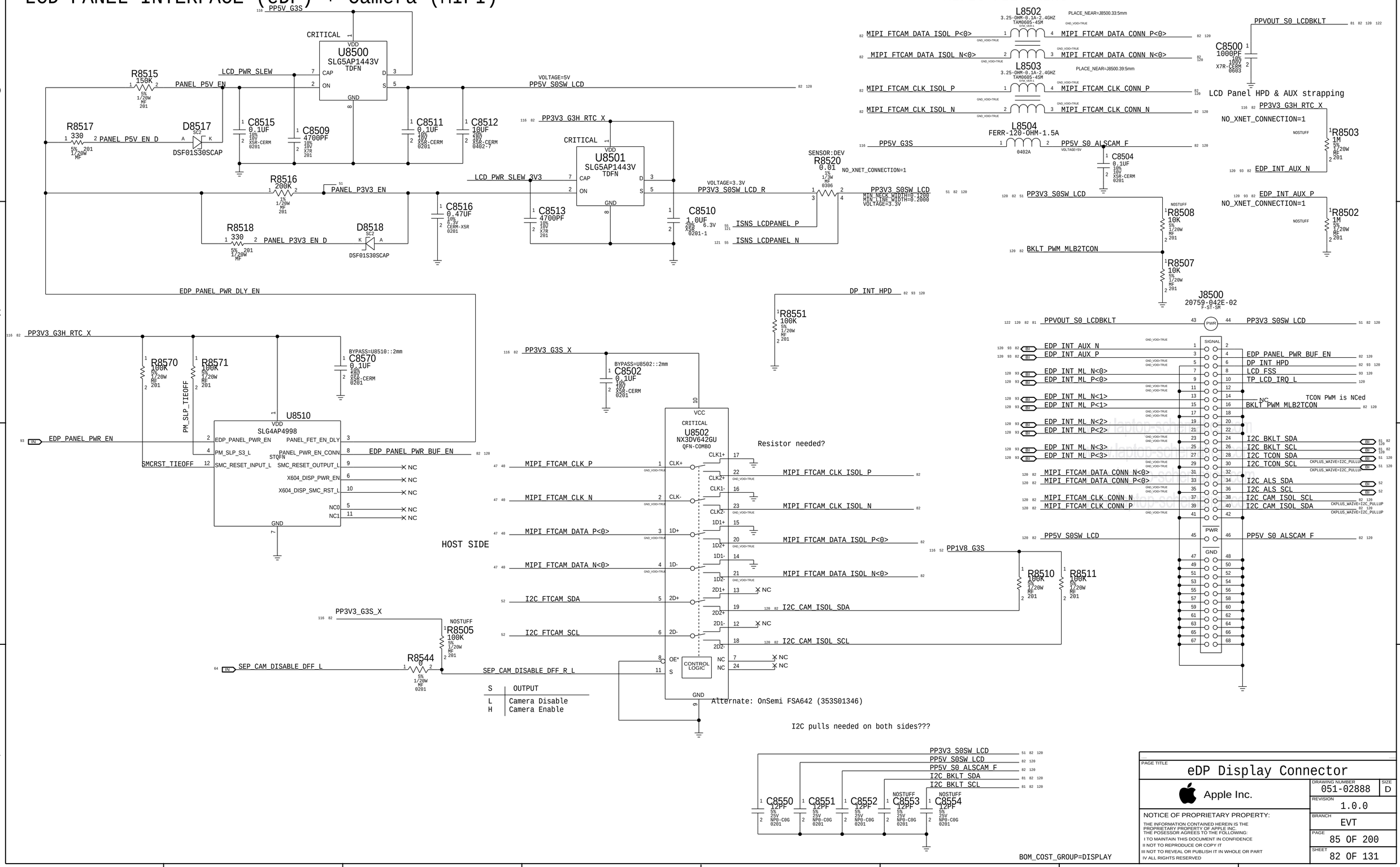
# LCD PANEL INTERFACE (eDP) + Camera (MIPI)




PAGE TITLE
## eDP Display Connector

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PAGE 85 OF 200
SHEET 82 OF 131

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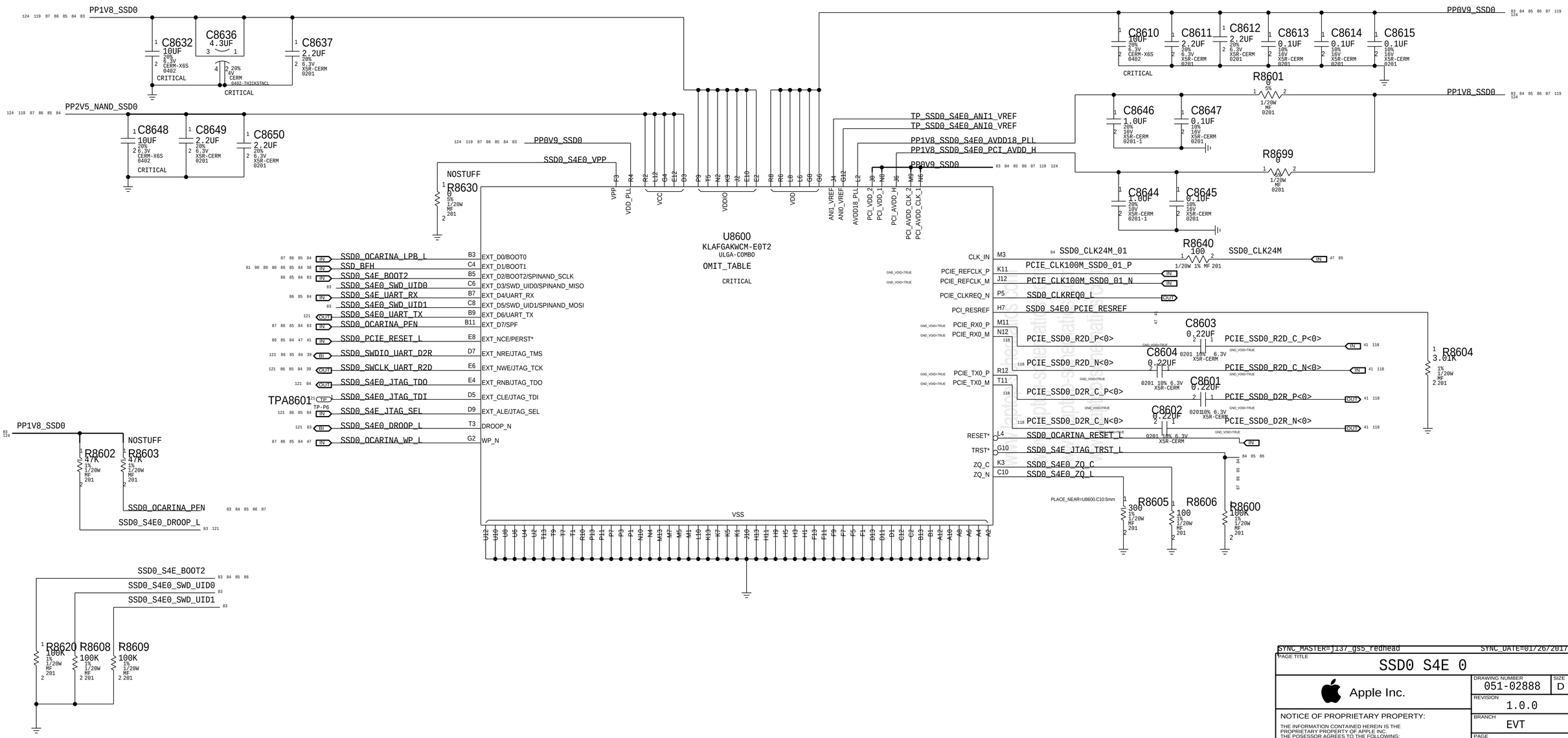
# S4E0




BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE

SSD0 S4E 0

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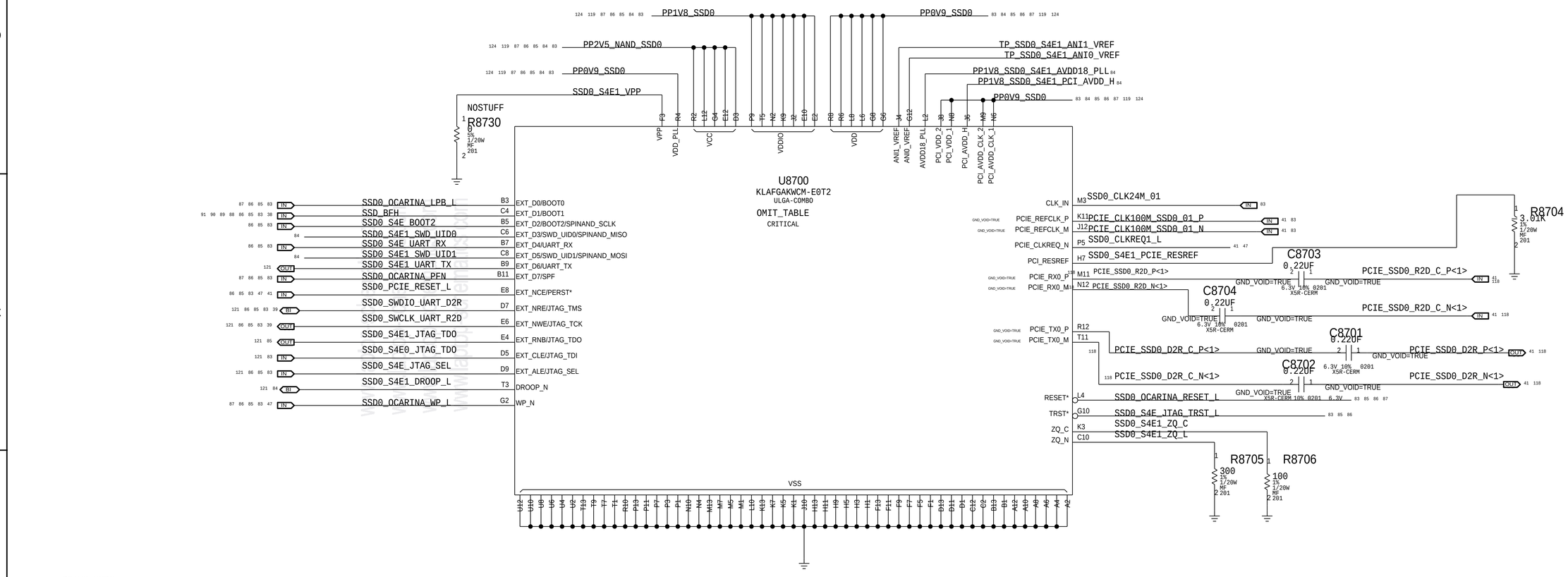
REVISION 1.0.0

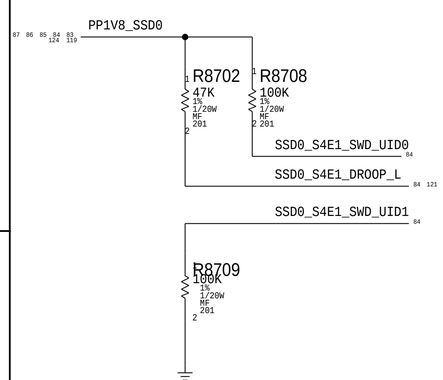
BRANCH EVT

PAGE 86 OF 200

SHEET 83 OF 131

# S4E1

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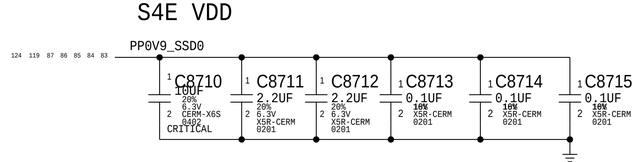
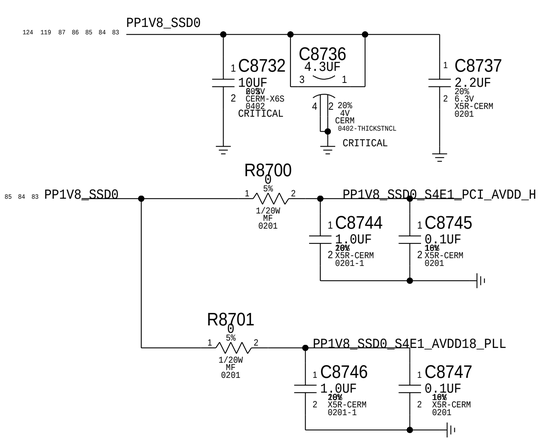



## S4E VDDIO

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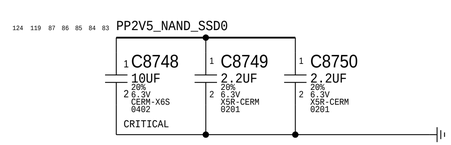


BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE
SSD0 S4E 1

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 87 OF 200
SHEET 84 OF 131

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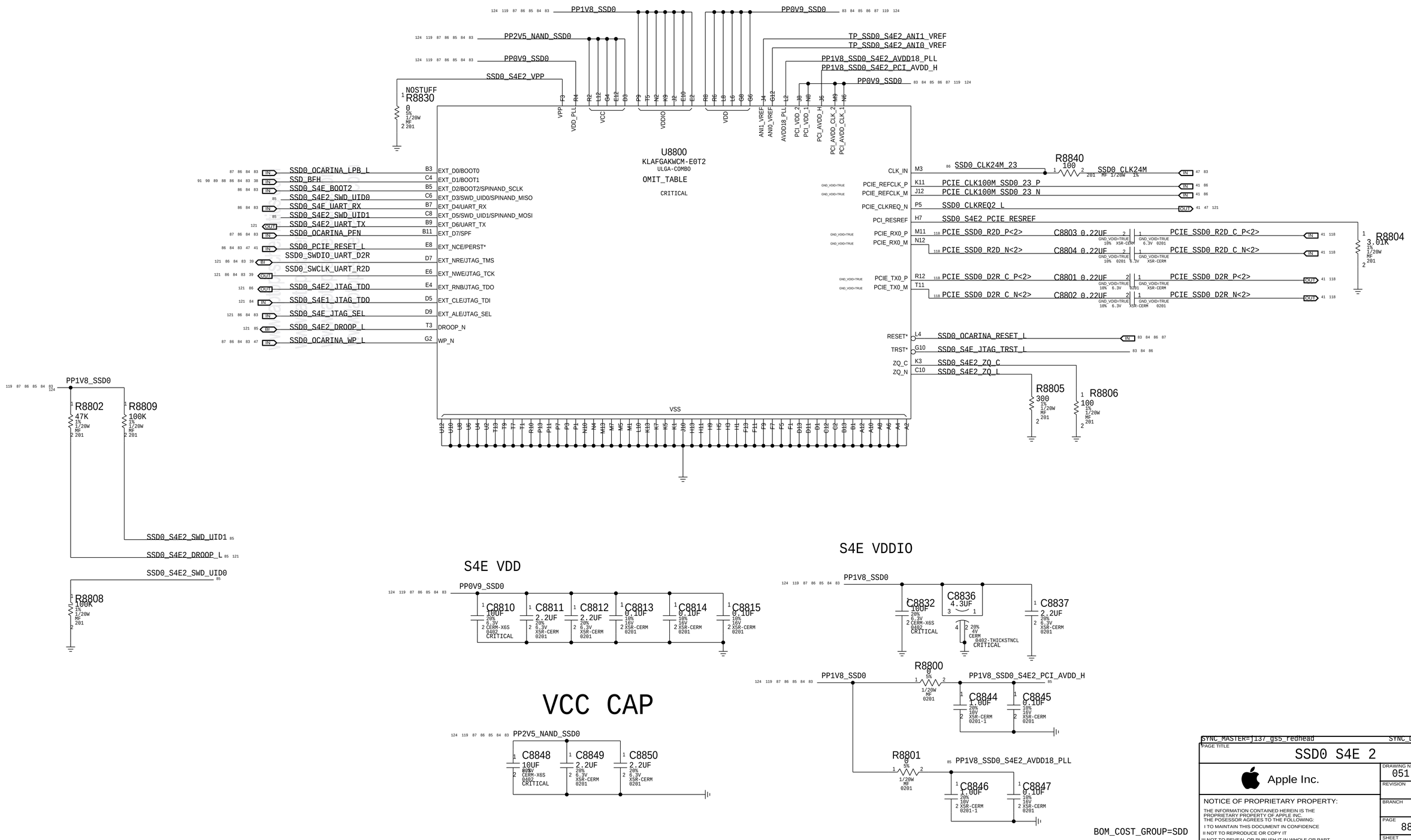


SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE
SSD0 S4E 2

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 88 OF 200
SHEET 85 OF 131

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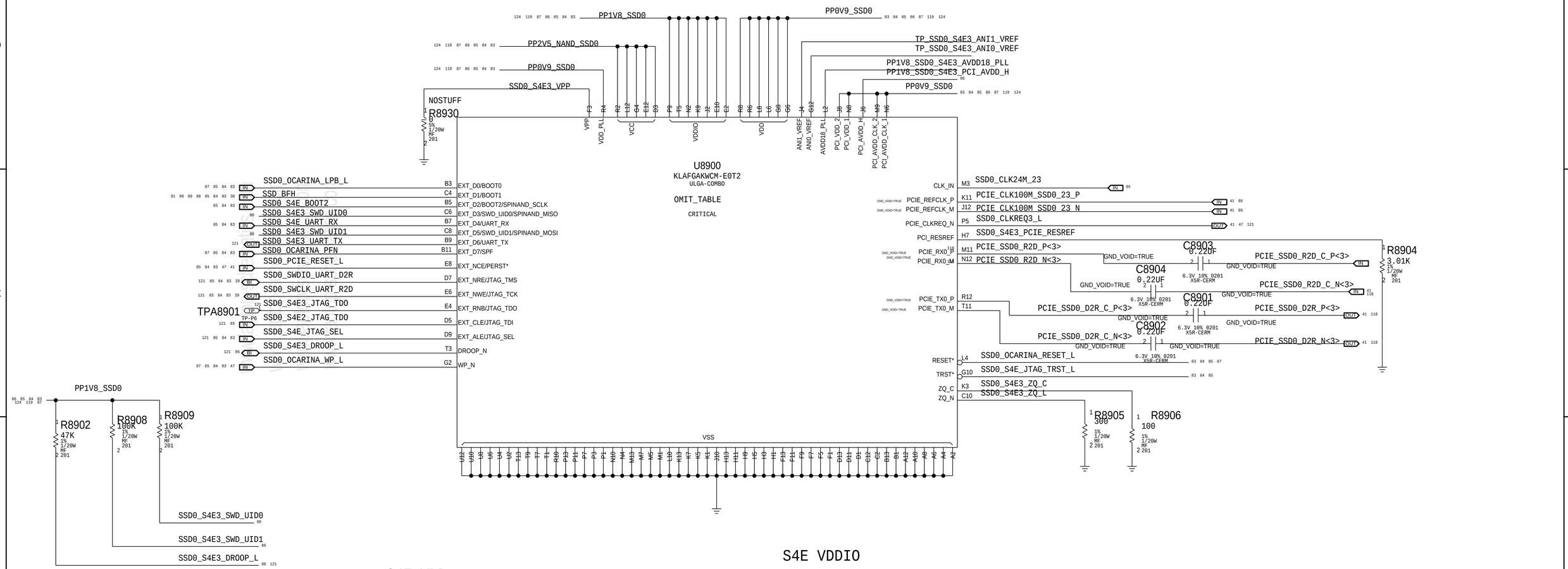


SYNC_MASTER=J137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 S4E 3

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0

BRANCH: EVT

PAGE: 89 OF 200

SHEET: 86 OF 131

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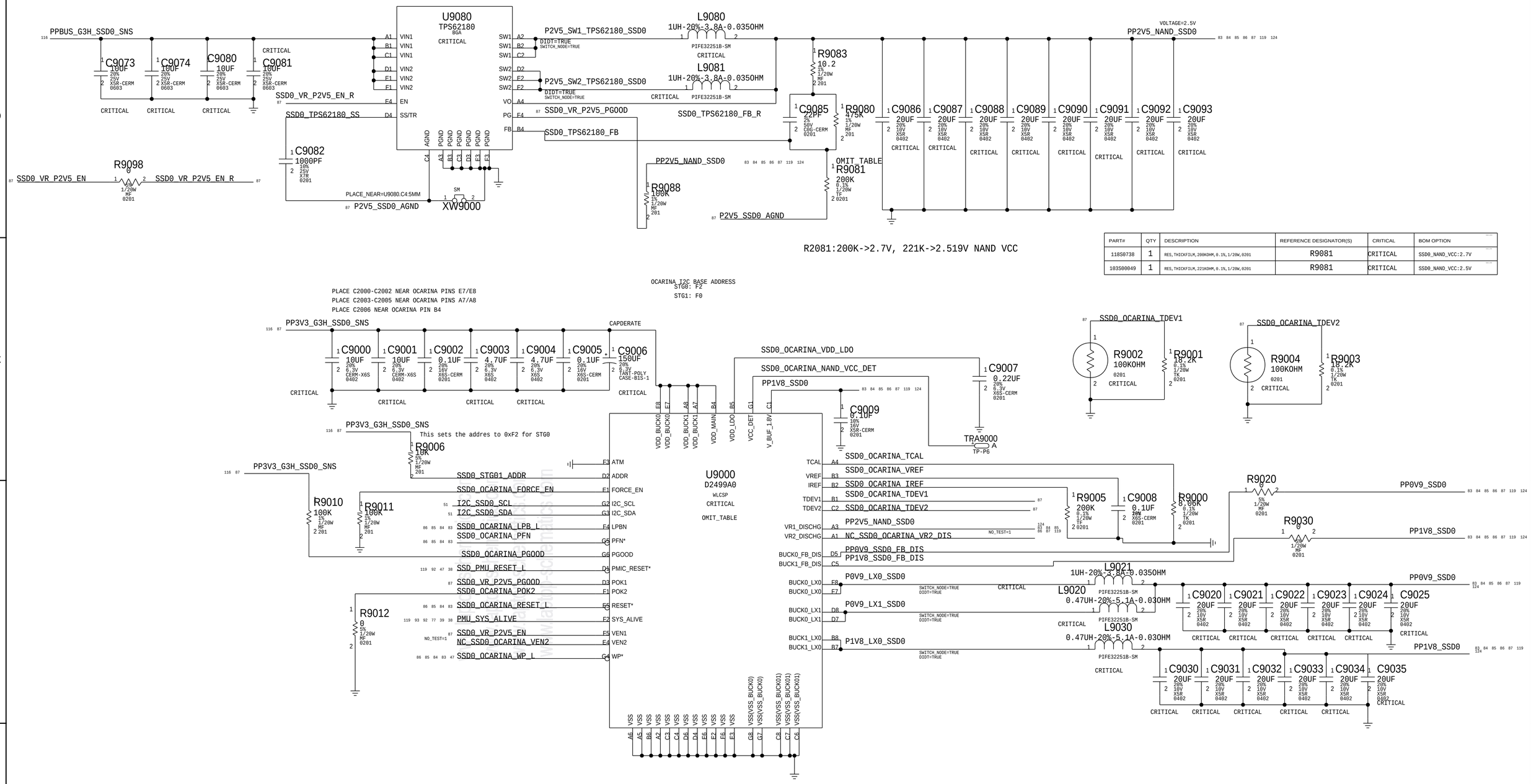


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 118S0738 | 1 | RES,THICKFILM,200KOHM,0.1%,1/20W,0201 | R9081 | CRITICAL | SSD0_NAND_VCC:2.7V |
| 103S00049 | 1 | RES,THICKFILM,221KOHM,0.1%,1/20W,0201 | R9081 | CRITICAL | SSD0_NAND_VCC:2.5V |

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 PMIC & VR

Apple Inc.

DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0

BRANCH: EVT

PAGE: 90 OF 200

SHEET: 87 OF 131

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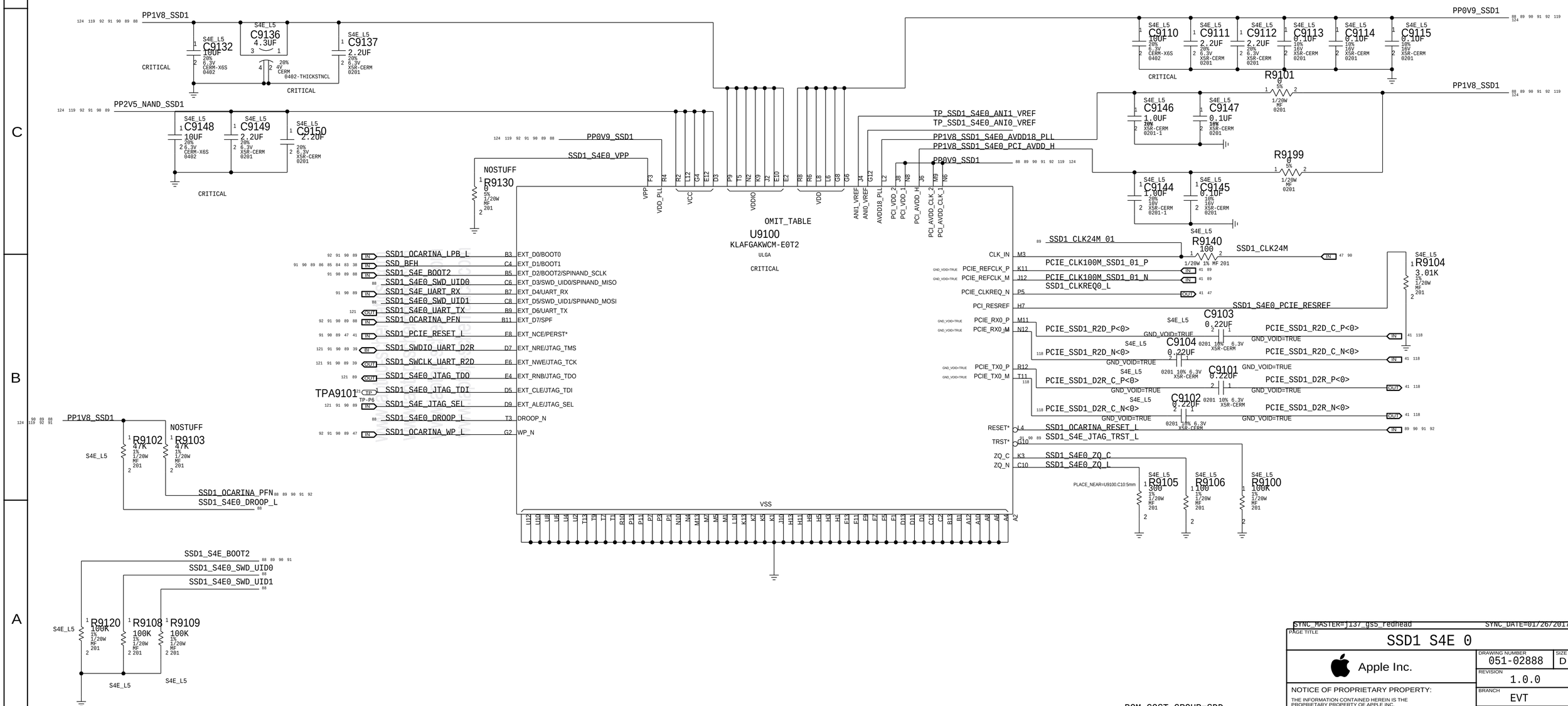
# S4E0

## VCC CAP




BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD1 S4E 0

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DRAWING NUMBER: 051-02888 SIZE: D

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PAGE: 91 OF 200

SHEET: 88 OF 131

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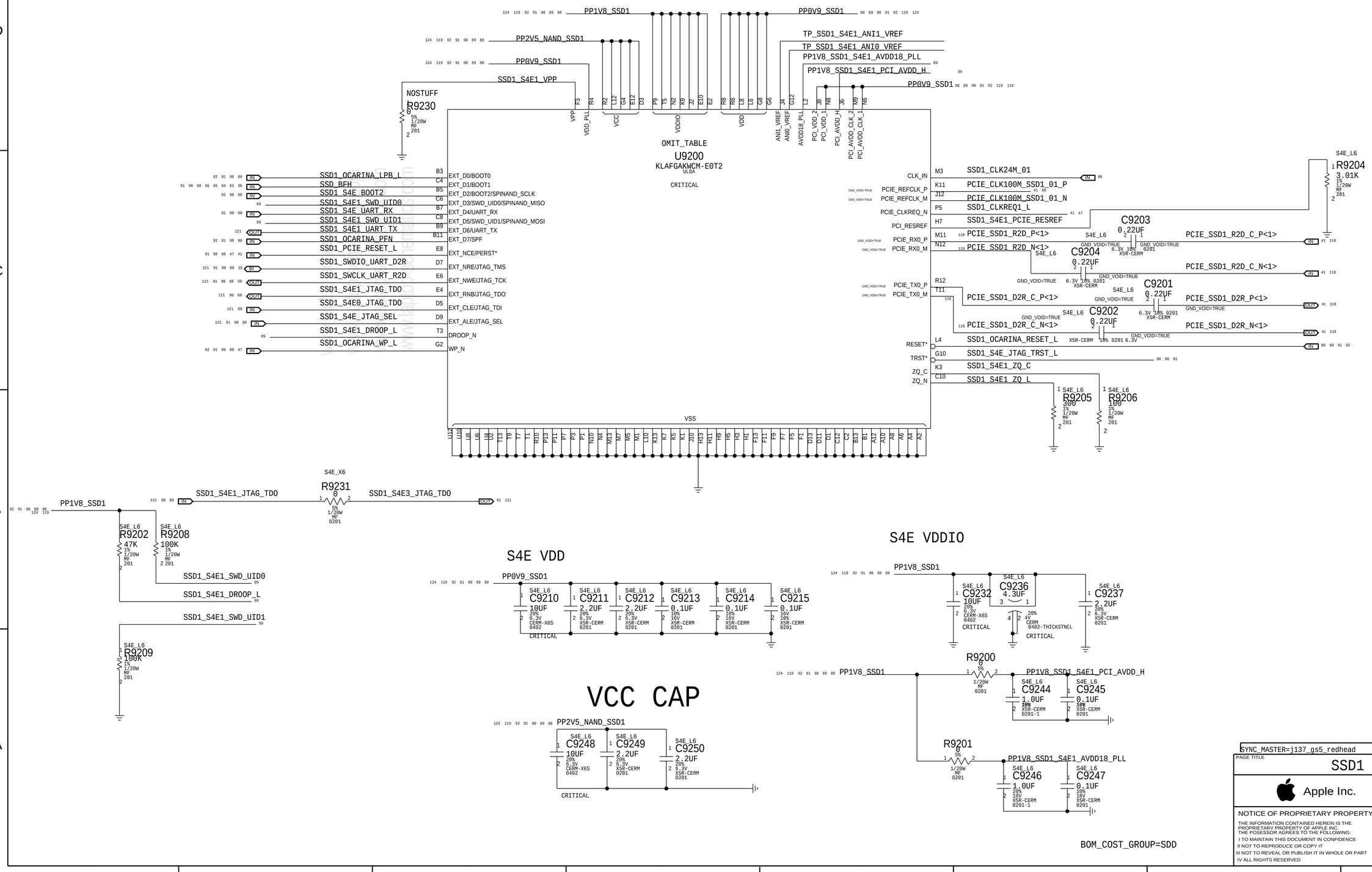
# S4E1

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PAGE TITLE: SSD1 S4E 1

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DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0

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SHEET: 89 OF 131

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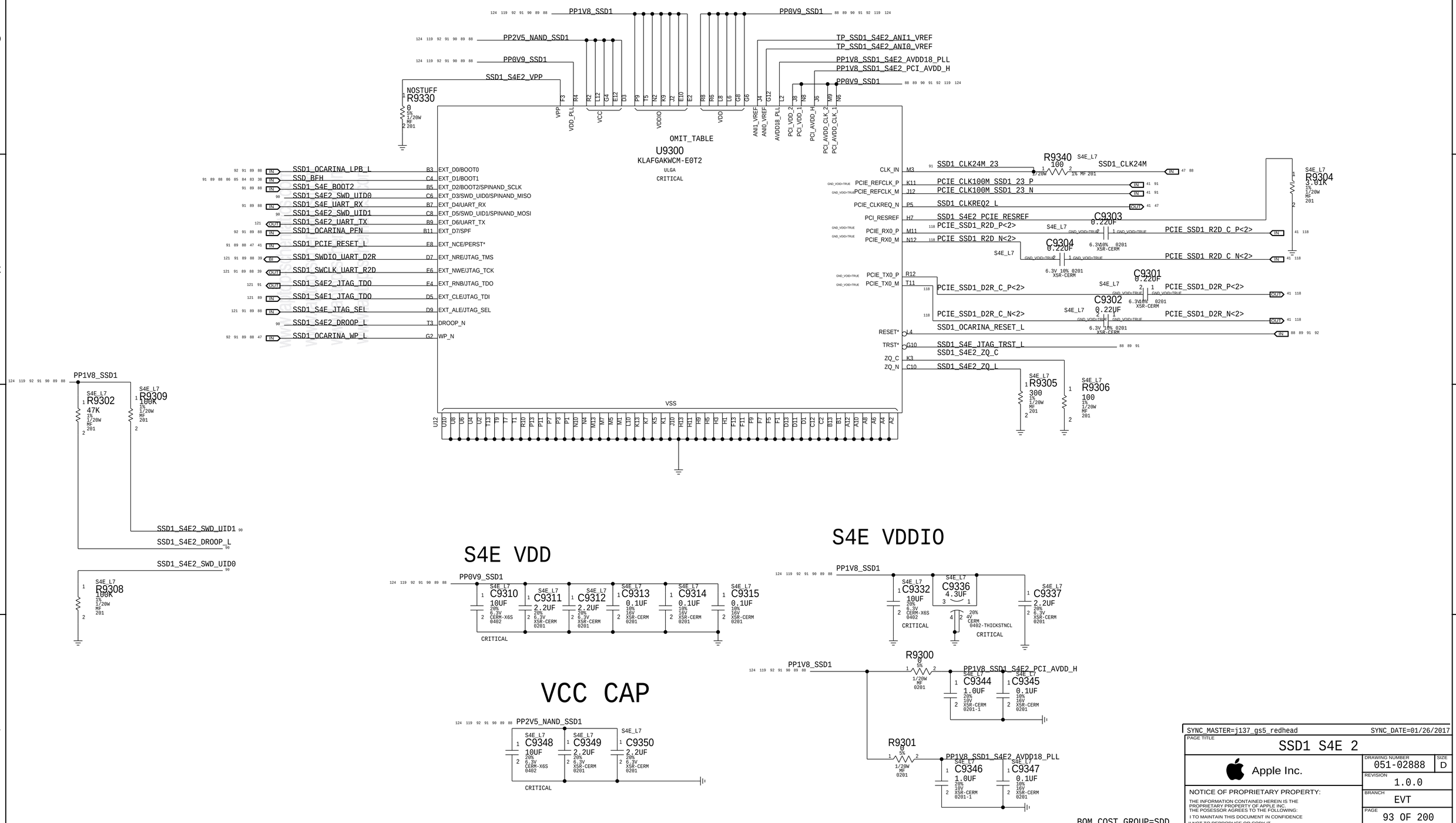
# S4E2




SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE
SSD1 S4E 2

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PAGE 93 OF 200
SHEET 90 OF 131

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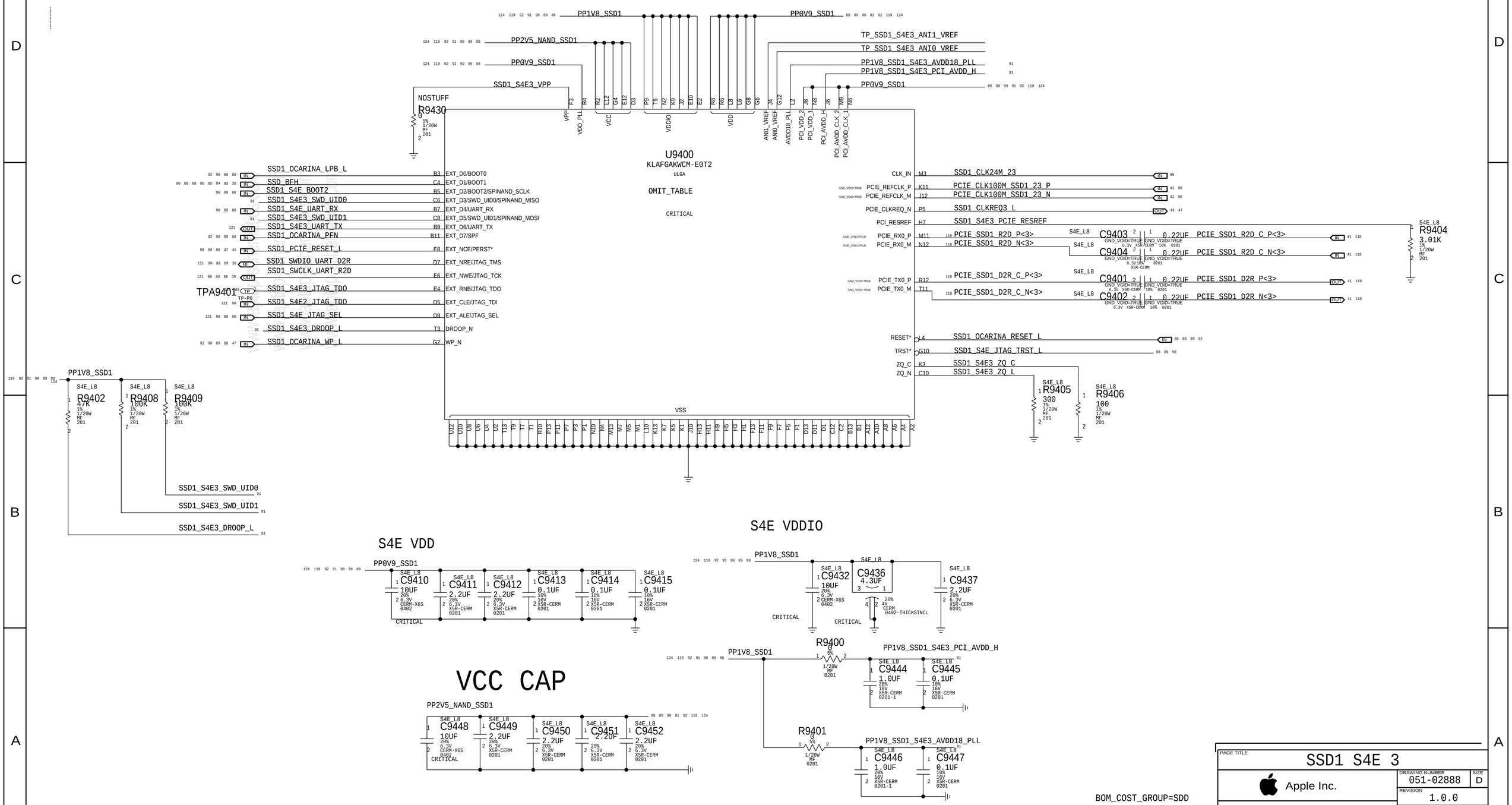
# S4E3

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| PAGE TITLE | SSD1 S4E 3 |
| Apple Inc. | |
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
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| PAGE | 94 OF 200 |
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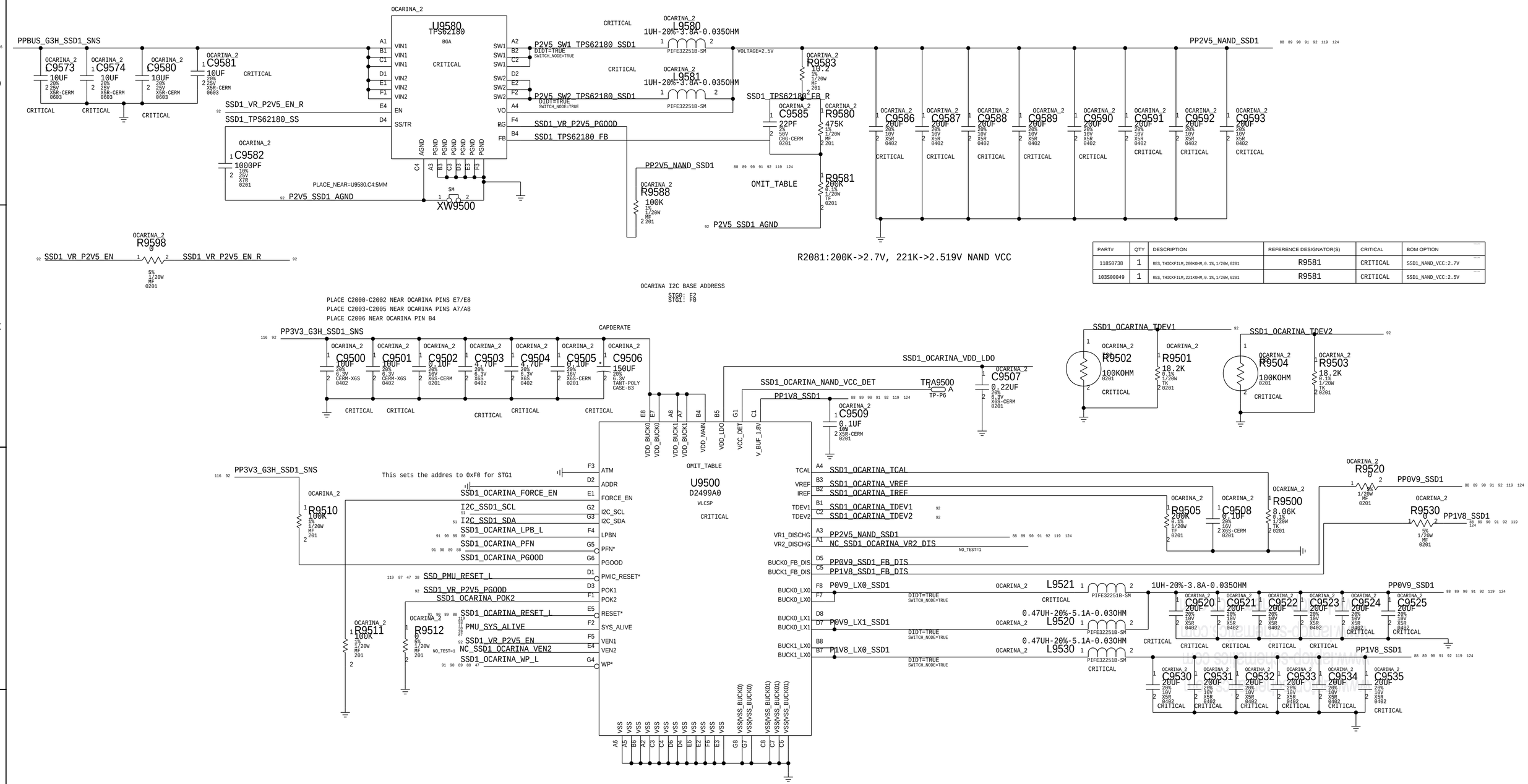


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
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| 118S0738 | 1 | RES,THICKFILM,200KOHM,0.1%,1/20W,0201 | R9581 | CRITICAL | SSD1_NAND_VCC:2.7V |
| 103S00049 | 1 | RES,THICKFILM,221KOHM,0.1%,1/20W,0201 | R9581 | CRITICAL | SSD1_NAND_VCC:2.5V |

PAGE TITLE
SSD1 PMIC & VR

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PAGE 95 OF 200
SHEET 92 OF 131

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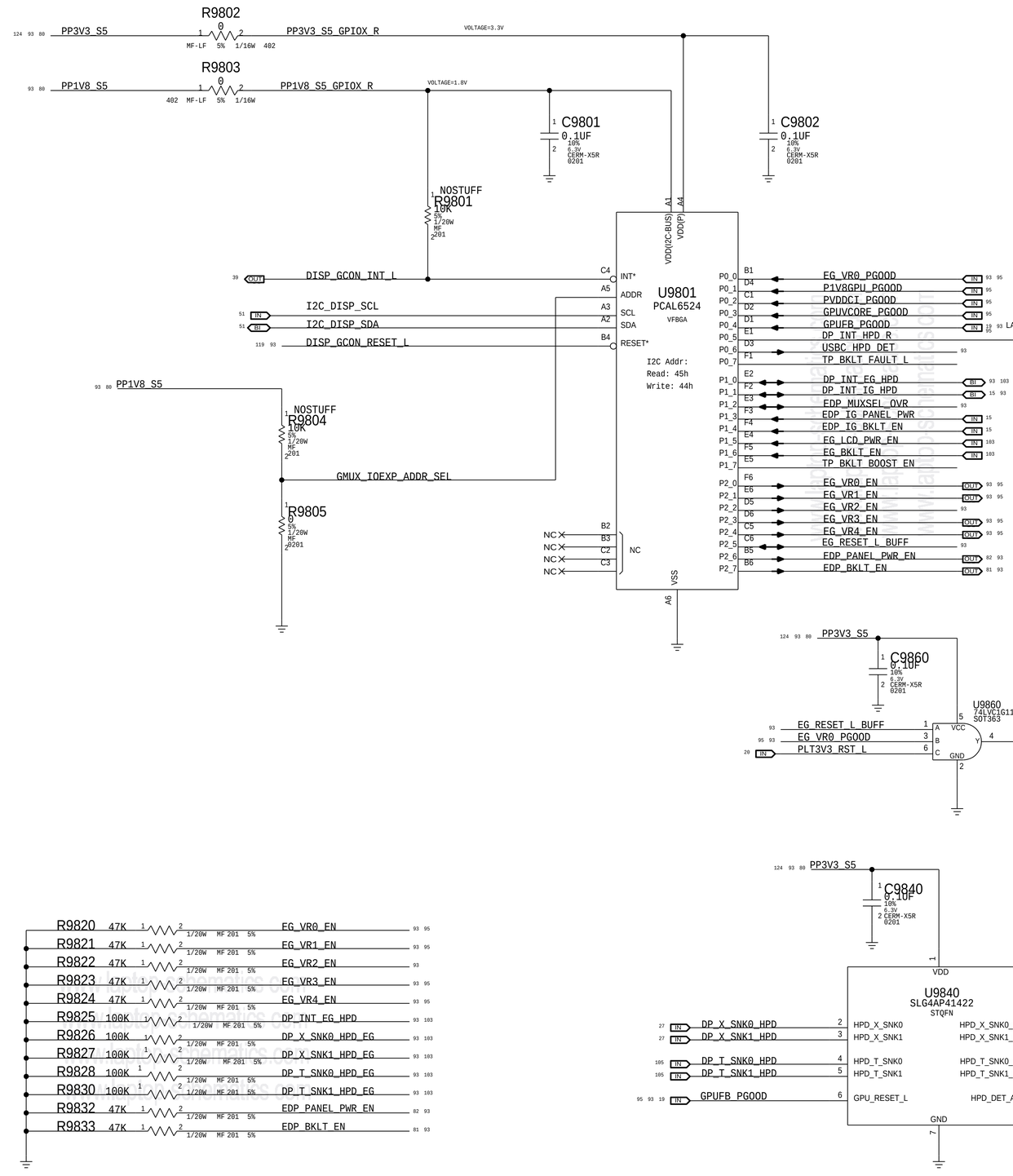
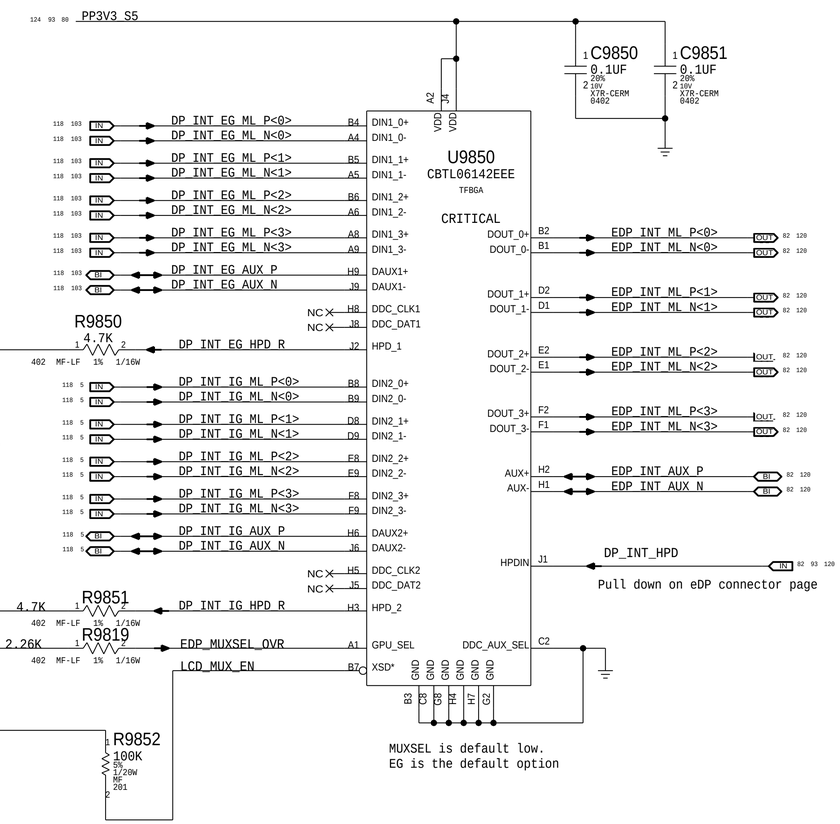
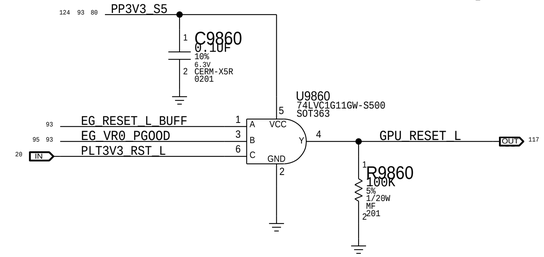
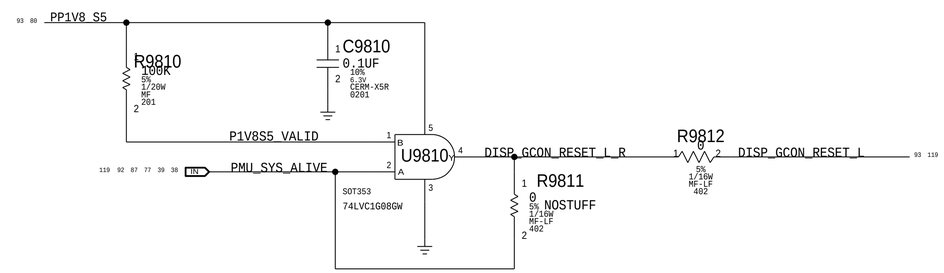
# GMUX GPIO Expander

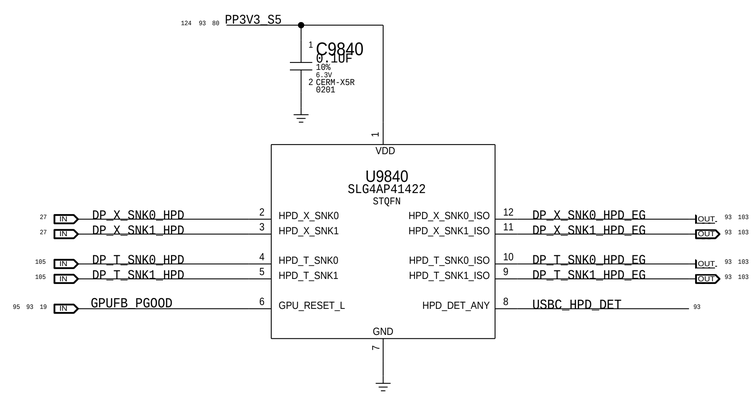



# DP 2:1 ANALOG MUX







BOM_COST_GROUP=GRAPHICS

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REVISION: 1.0.0

BRANCH: EVT

PAGE: 98 OF 200

SHEET: 93 OF 131

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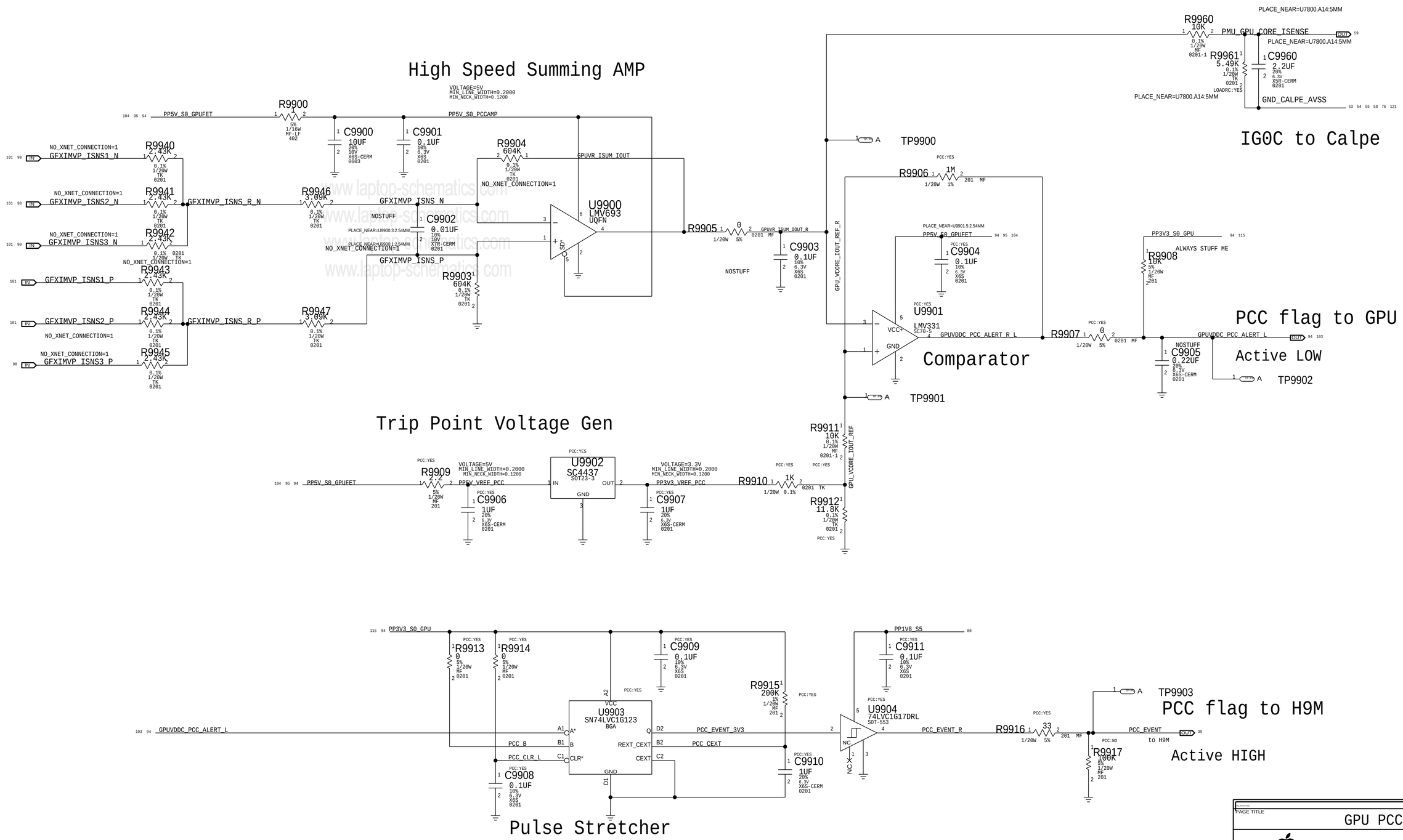
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 117S0008 | 1 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | R9961 | | LOADRC:NO |




PAGE TITLE

# GPU PCC

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PAGE 99 OF 200

SHEET 94 OF 131

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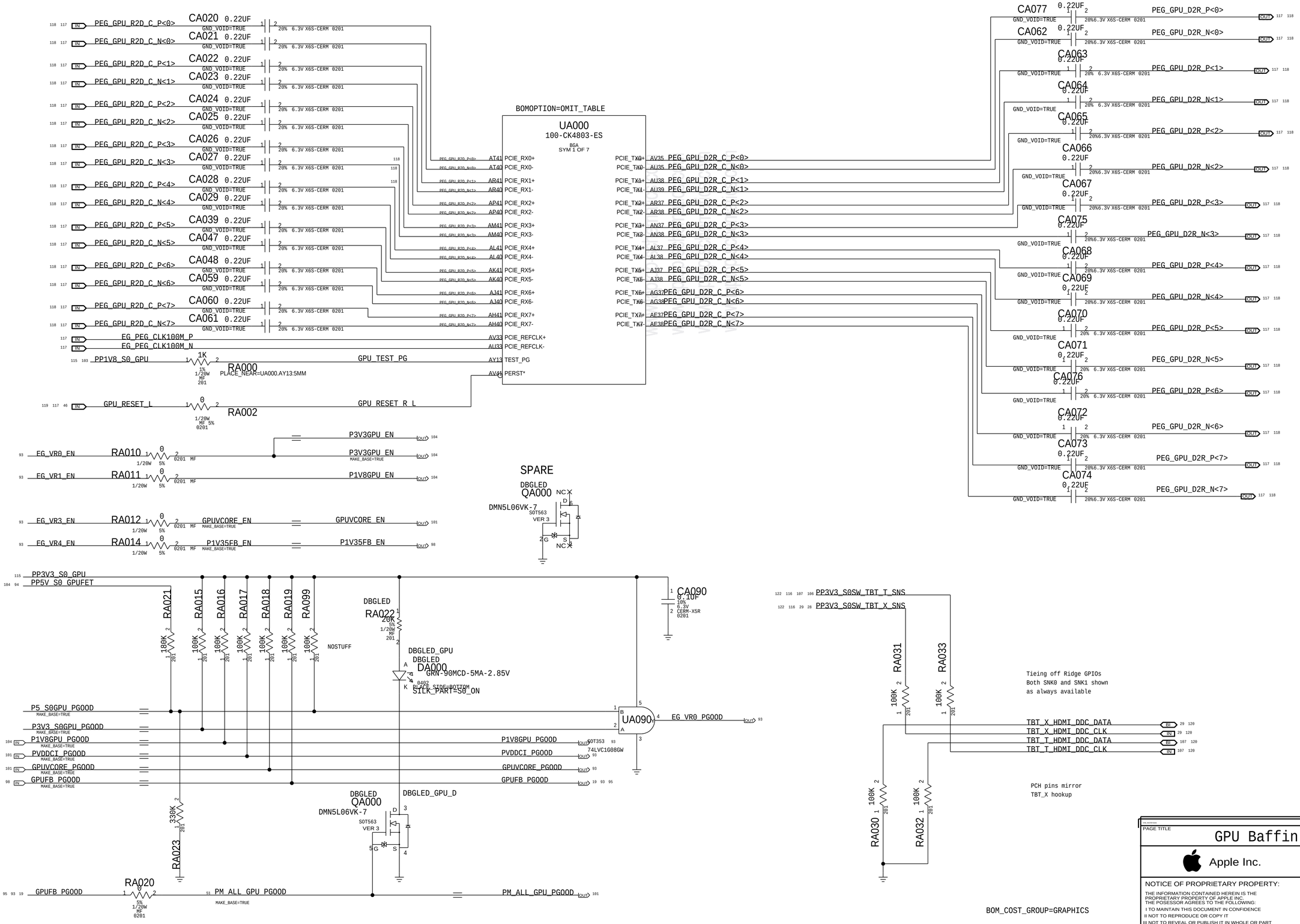


PAGE TITLE

# GPU Baffin PCIe

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BRANCH 100 OF 200

PAGE

SHEET 95 OF 131

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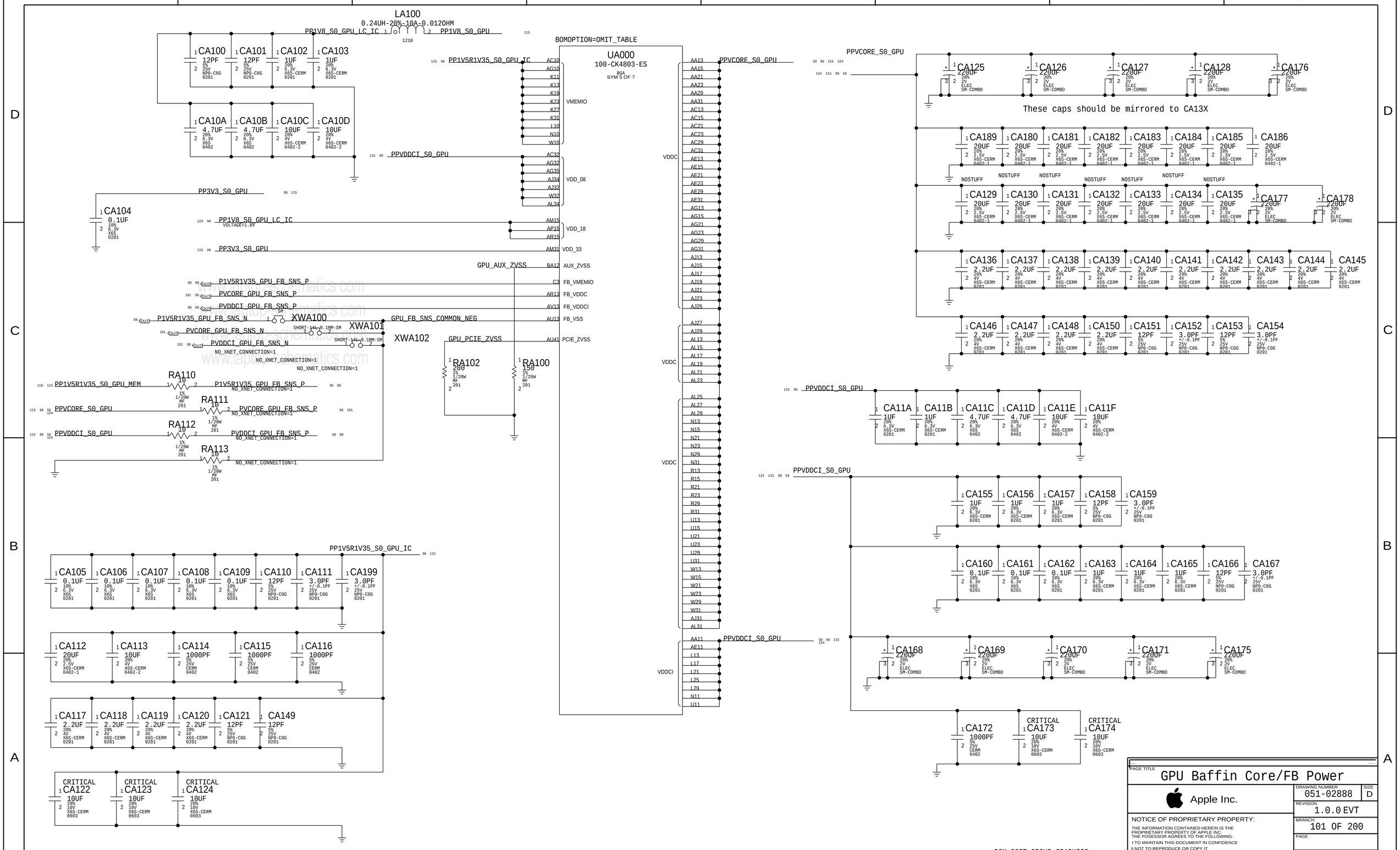


PAGE TITLE
# GPU Baffin Core/FB Power

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BRANCH 101 OF 200
PAGE
SHEET 96 OF 131

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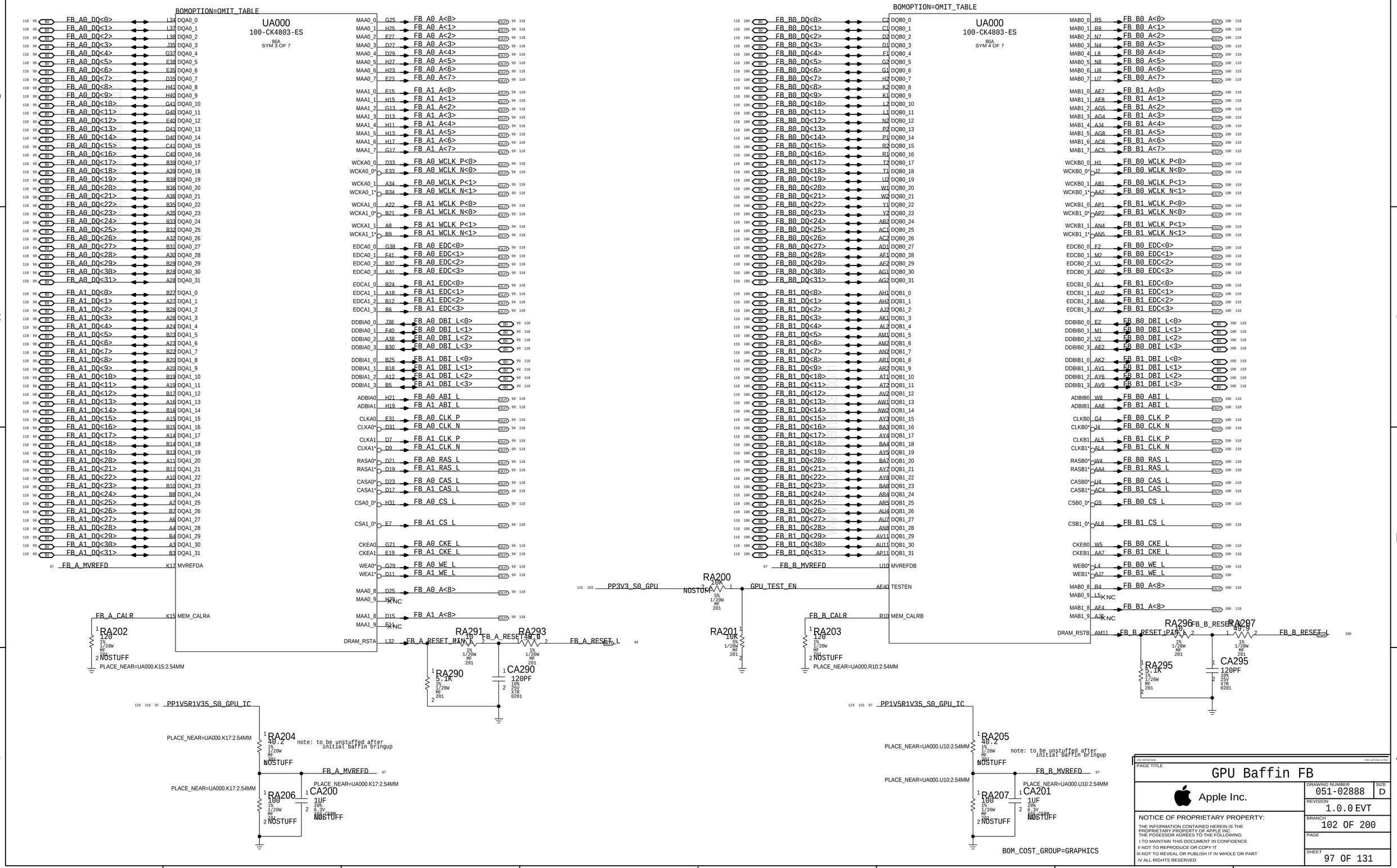


PAGE TITLE

# GPU Baffin FB

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BRANCH 102 OF 200

PAGE

SHEET 97 OF 131

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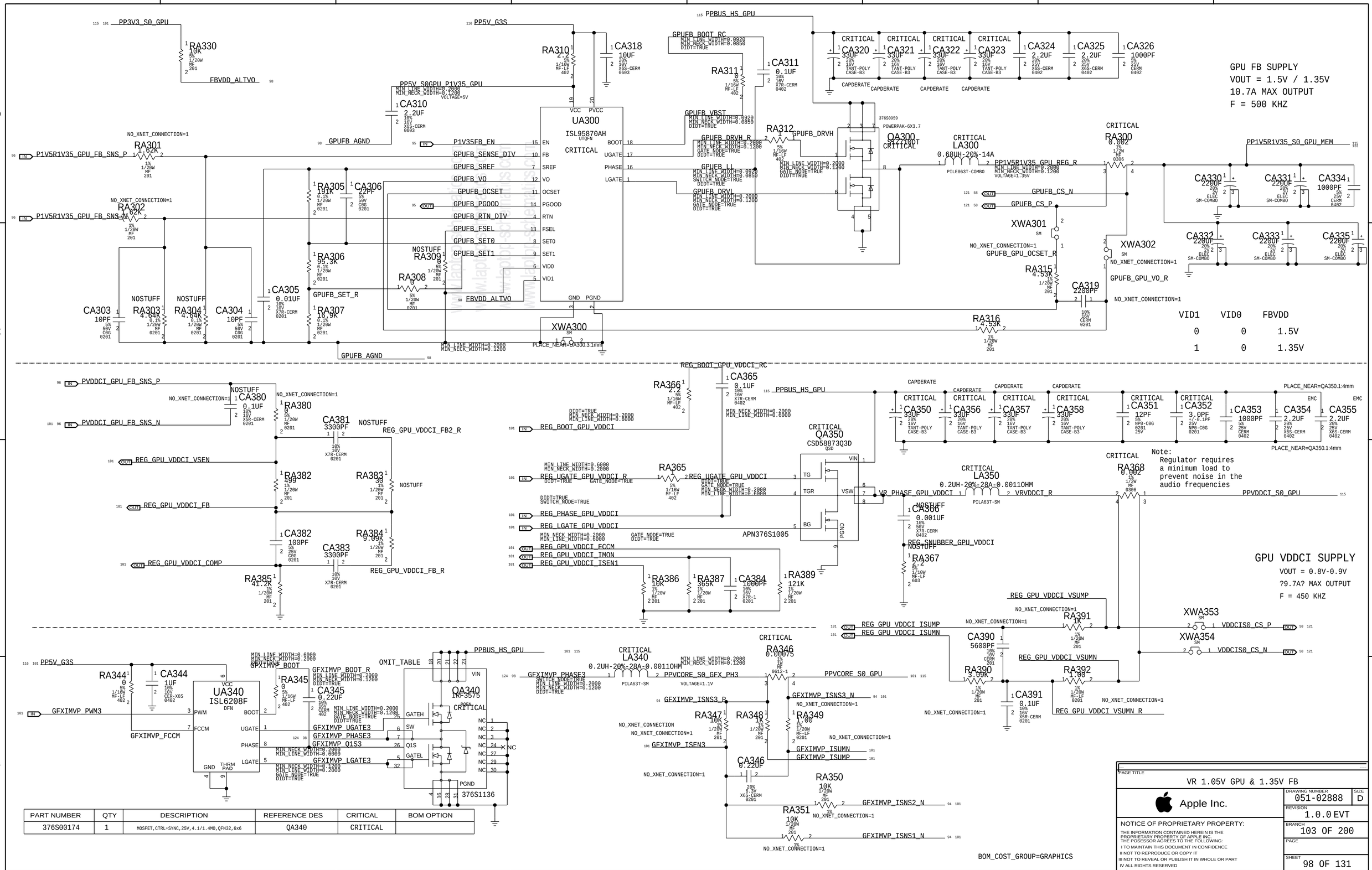


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 376S00174 | 1 | MOSFET,CTRL+SYNC,25V,4.1/1.4MO,QFN32,6x6 | QA340 | CRITICAL | |

PAGE TITLE
VR 1.05V GPU & 1.35V FB

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REVISION 1.0.0 EVT
BRANCH 103 OF 200
PAGE
SHEET 98 OF 131

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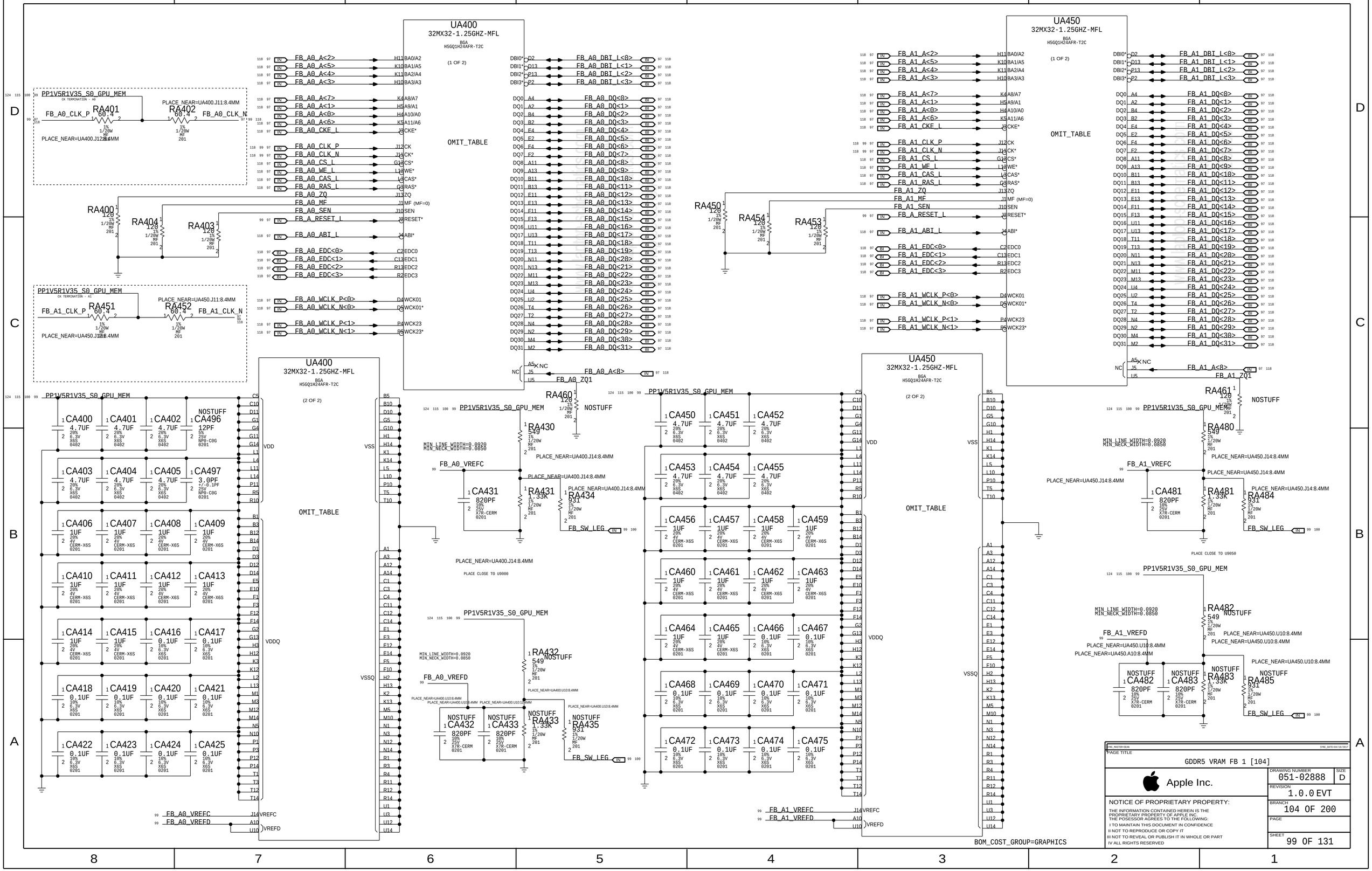


PAGE TITLE

GDDR5 VRAM FB 1 [104]

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BRANCH 104 OF 200

PAGE

SHEET 99 OF 131

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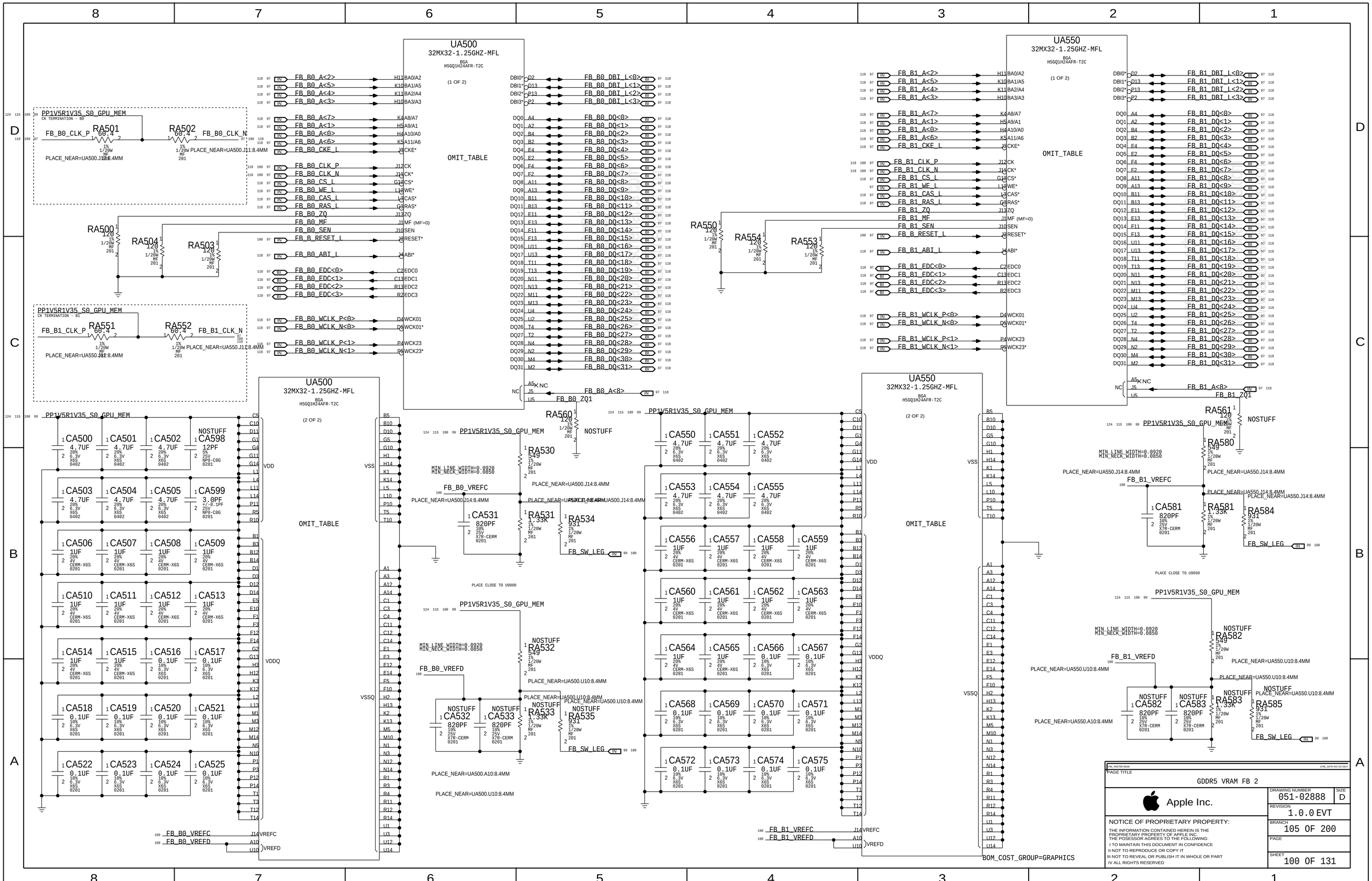


PAGE TITLE

GDDR5 VRAM FB 2

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BRANCH 105 OF 200

PAGE

SHEET 100 OF 131

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| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 376S00174 | 2 | MOSFET,CTRL+SYNC,25V,4.1/1.4MO,QFN32,6x6 | QA640,QA650 | CRITICAL | |

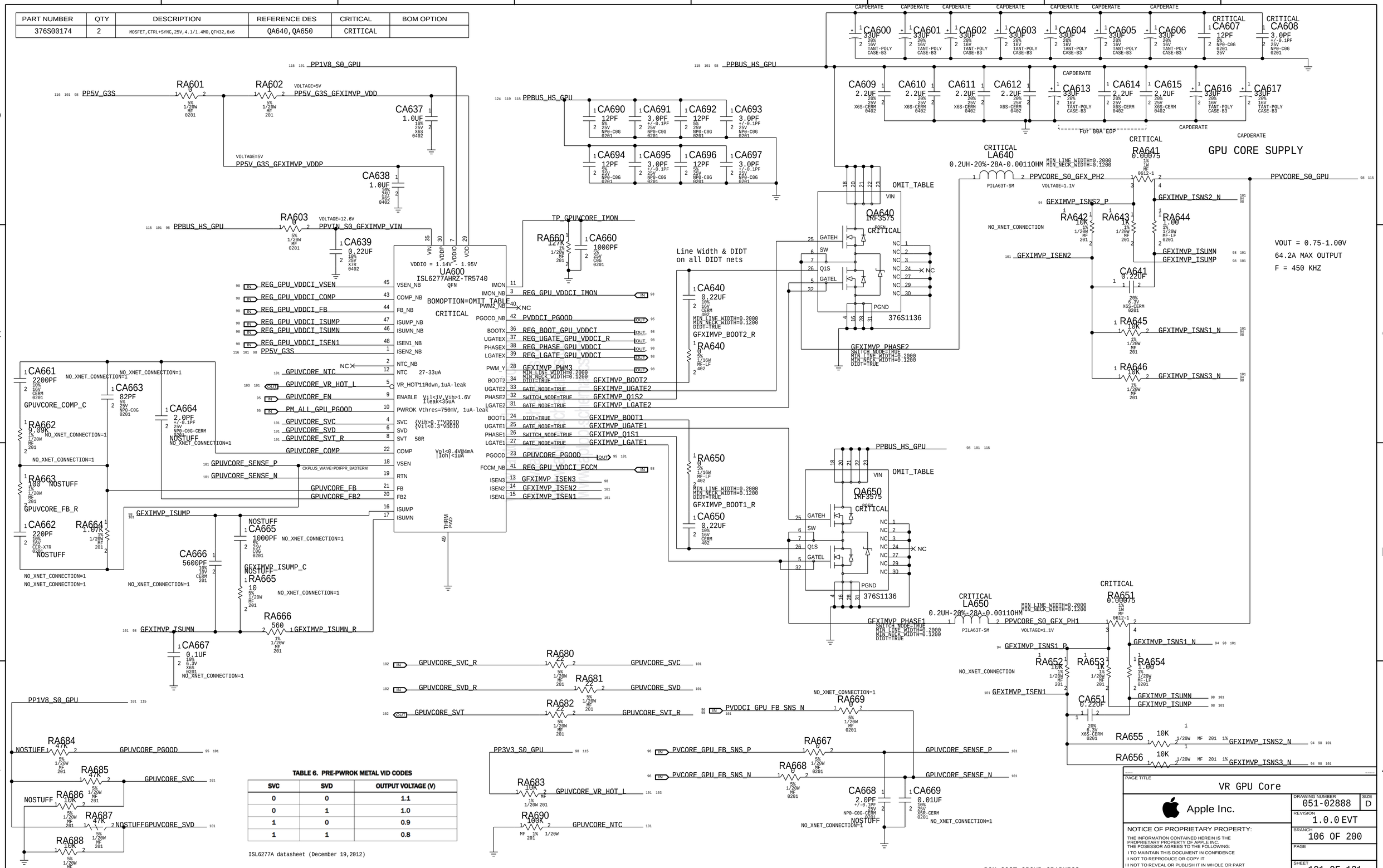


**TABLE 6. PRE-PWROK METAL VID CODES**

| SVC | SVD | OUTPUT VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 1.1 |
| 0 | 1 | 1.0 |
| 1 | 0 | 0.9 |
| 1 | 1 | 0.8 |

ISL6277A datasheet (December 19,2012)

PAGE TITLE
VR GPU Core

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0 EVT
BRANCH 106 OF 200
PAGE
SHEET 101 OF 131

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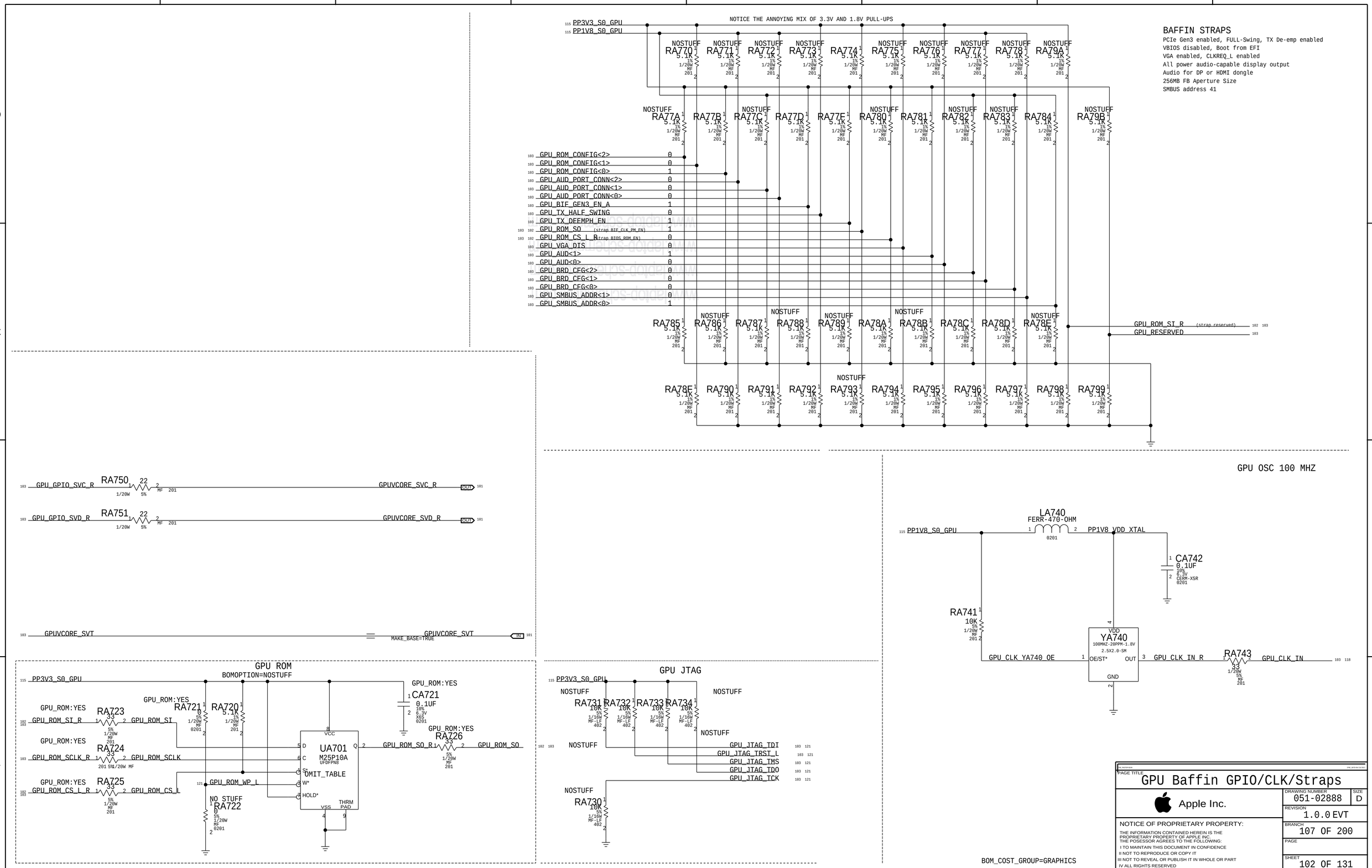


PAGE TITLE

# GPU Baffin GPIO/CLK/Straps

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DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 107 OF 200

PAGE

SHEET 102 OF 131

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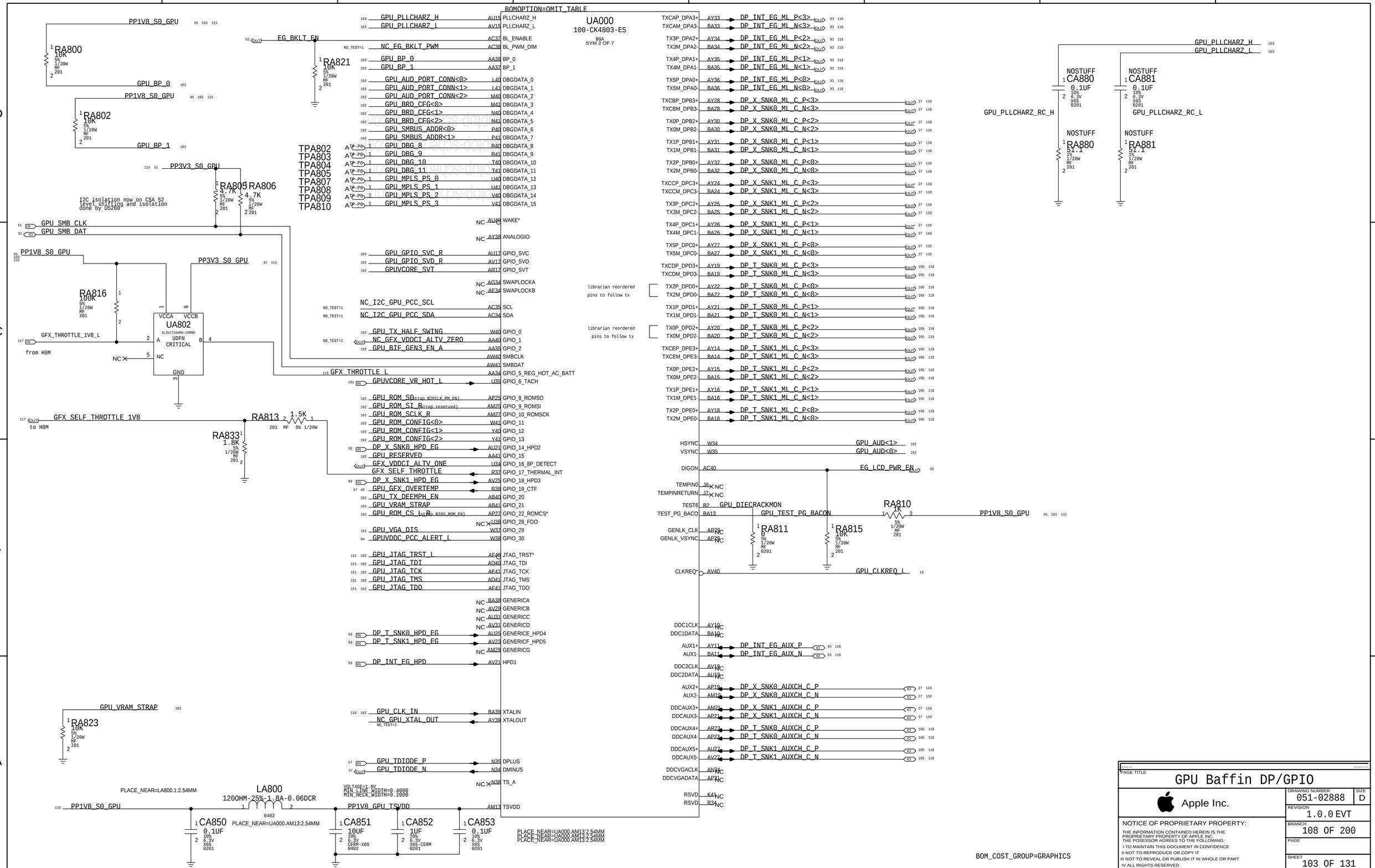
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RA800
10K
GPU_BP_0
RA821
EG_BKLT_EN
NC_EG_BKLT_PWM
RA802
GPU_BP_1
PP3V3_S0_GPU
RA805
RA806
4.7K
I2C isolation now on CSA 52 level shifting and isolation done by U5200
GPU_SMB_CLK
GPU_SMB_DAT
RA816
100K
UA802
SLSV1T344MU-COMBO
UDFN
CRITICAL
VCCA
VCCB
GND
GFX_THROTTLE_1V8_L
from H9M
GFX_SELF_THROTTLE_1V8
to H9M
RA813
1.5K
RA833
1.8K
GPU_VRAM_STRAP
RA823
10K
LA800
1200HM-25%-1.8A-0.06DCR
PLACE_NEAR=LA800.1:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PP1V8_GPU_TSVDD
CA850
0.1UF
CA851
10UF
CA852
1UF
CA853
0.1UF
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
GPU_PLLCHARZ_H
GPU_PLLCHARZ_L
NOSTUFF
CA880
CA881
0.1UF
GPU_PLLCHARZ_RC_H
GPU_PLLCHARZ_RC_L
RA880
RA881
51.1
PLL_H
PLL_L
BL_ENABLE
BL_PWM_DIM
BP_0
BP_1
DBGDATA_0
DBGDATA_1
DBGDATA_2
DBGDATA_3
DBGDATA_4
DBGDATA_5
DBGDATA_6
DBGDATA_7
DBGDATA_8
DBGDATA_9
DBGDATA_10
DBGDATA_11
DBGDATA_12
DBGDATA_13
DBGDATA_14
DBGDATA_15
TPA802
TPA803
TPA804
TPA805
TPA807
TPA808
TPA809
TPA810
WAKE*
ANALOGIO
GPIO_SVC
GPIO_SVD
GPIO_SVT
SWAPLOCKA
SWAPLOCKB
SCL
SDA
GPIO_0
GPIO_1
GPIO_2
SMBCLK
SMBDAT
GPIO_5_REG_HOT_AC_BATT
GPIO_6_TACH
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15
GPIO_16_8P_DETECT
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20
GPIO_21
GPIO_22_ROMCS*
GPIO_28_FDO
GPIO_29
GPIO_30
JTAG_TRST*
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG
HPD1
XTALIN
XTALOUT
DPLUS
DMINUS
TS_A
TSVDD
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GPU_DIECRACKMON
GPU_TEST_PG_BACON
RA810
1K
PP1V8_S0_GPU
RA811
0
RA815
10K
GPU_CLKREQ_L
DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_X_SNK0_AUXCH_C_P
DP_X_SNK0_AUXCH_C_N
DP_X_SNK1_AUXCH_C_P
DP_X_SNK1_AUXCH_C_N
DP_T_SNK0_AUXCH_C_P
DP_T_SNK0_AUXCH_C_N
DP_T_SNK1_AUXCH_C_P
DP_T_SNK1_AUXCH_C_N
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
GPU Baffin DP/GPIO
Apple Inc.
DRAWING NUMBER
051-02888
SIZE
D
REVISION
1.0.0 EVT
BRANCH
108 OF 200
PAGE
SHEET
103 OF 131
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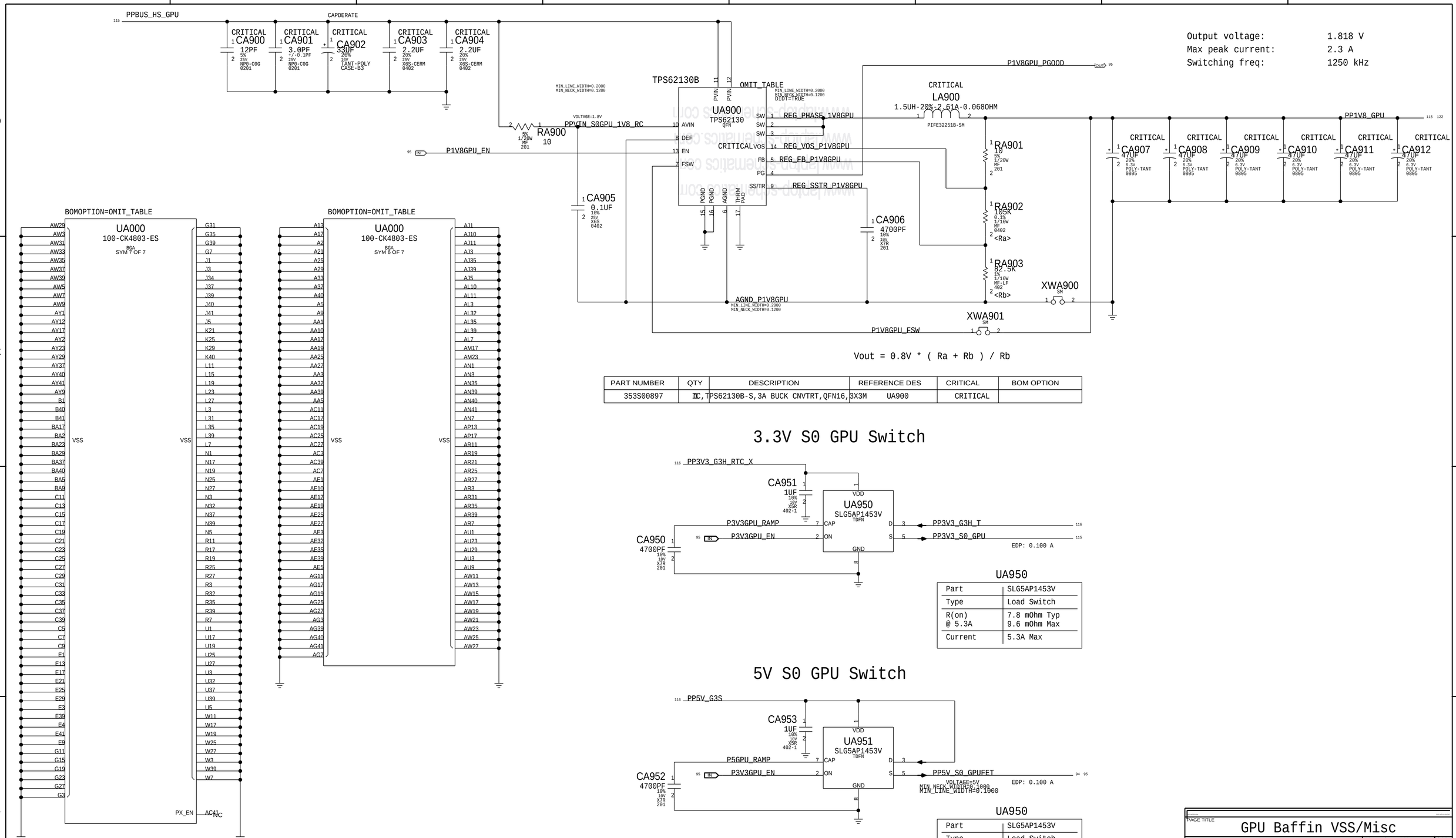


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 353S00897 | 1 | IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M | UA900 | CRITICAL | |

## 3.3V S0 GPU Switch

UA950

| | |
|---|---|
| Part | SLG5AP1453V |
| Type | Load Switch |
| R(on) @ 5.3A | 7.8 mOhm Typ<br>9.6 mOhm Max |
| Current | 5.3A Max |

## 5V S0 GPU Switch

UA950

| | |
|---|---|
| Part | SLG5AP1453V |
| Type | Load Switch |
| R(on) @ 5.3A | 7.8 mOhm Typ<br>9.6 mOhm Max |
| Current | 5.3A Max |

PAGE TITLE
GPU Baffin VSS/Misc

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0 EVT
BRANCH 109 OF 200
PAGE
SHEET 104 OF 131

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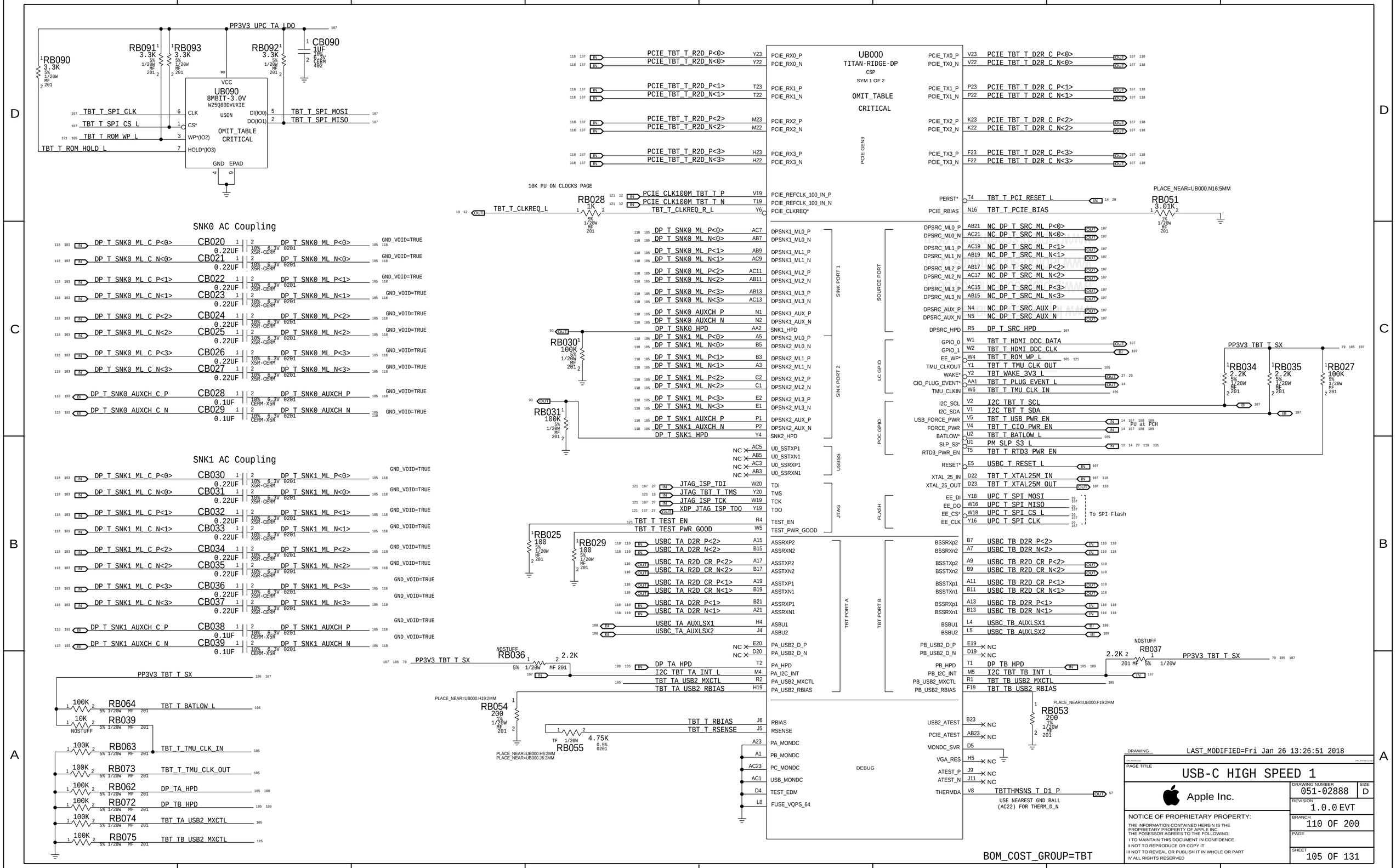
PP3V3_UPC_TA_LDO
RB090 3.3K
RB091 3.3K
RB093 3.3K
RB092 3.3K
CB090 1UF
UB090 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_ROM_WP_L
TBT_T_ROM_HOLD_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
UB000 TITAN-RIDGE-DP CSP SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
TBT_T_CLKREQ_L
RB028 1K
PLACE_NEAR=UB000.N16:5MM
RB051 3.01K
RB030 100K
RB031 100K
SINK PORT 1
SINK PORT 2
SOURCE PORT
LC GPIO
POC GPIO
USBSS
JTAG
FLASH
To SPI Flash
PU at PCH
RB025 100
RB029 100
TBT PORT A
TBT PORT B
NOSTUFF
RB036 2.2K
PP3V3_TBT_T_SX
RB037 2.2K
RB054 200
RB055 4.75K
RB053 200
DEBUG
USE NEAREST GND BALL (AC22) FOR THERM_D_N
RB064 100K
RB039 10K
RB063 100K
RB073 100K
RB062 100K
RB072 100K
RB074 100K
RB075 100K
RB034 2.2K
RB035 2.2K
RB027 100K
BOM_COST_GROUP=TBT
DRAWING
LAST_MODIFIED=Fri Jan 26 13:26:51 2018
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER
051-02888
SIZE
D
REVISION
1.0.0 EVT
BRANCH
110 OF 200
PAGE
SHEET
105 OF 131
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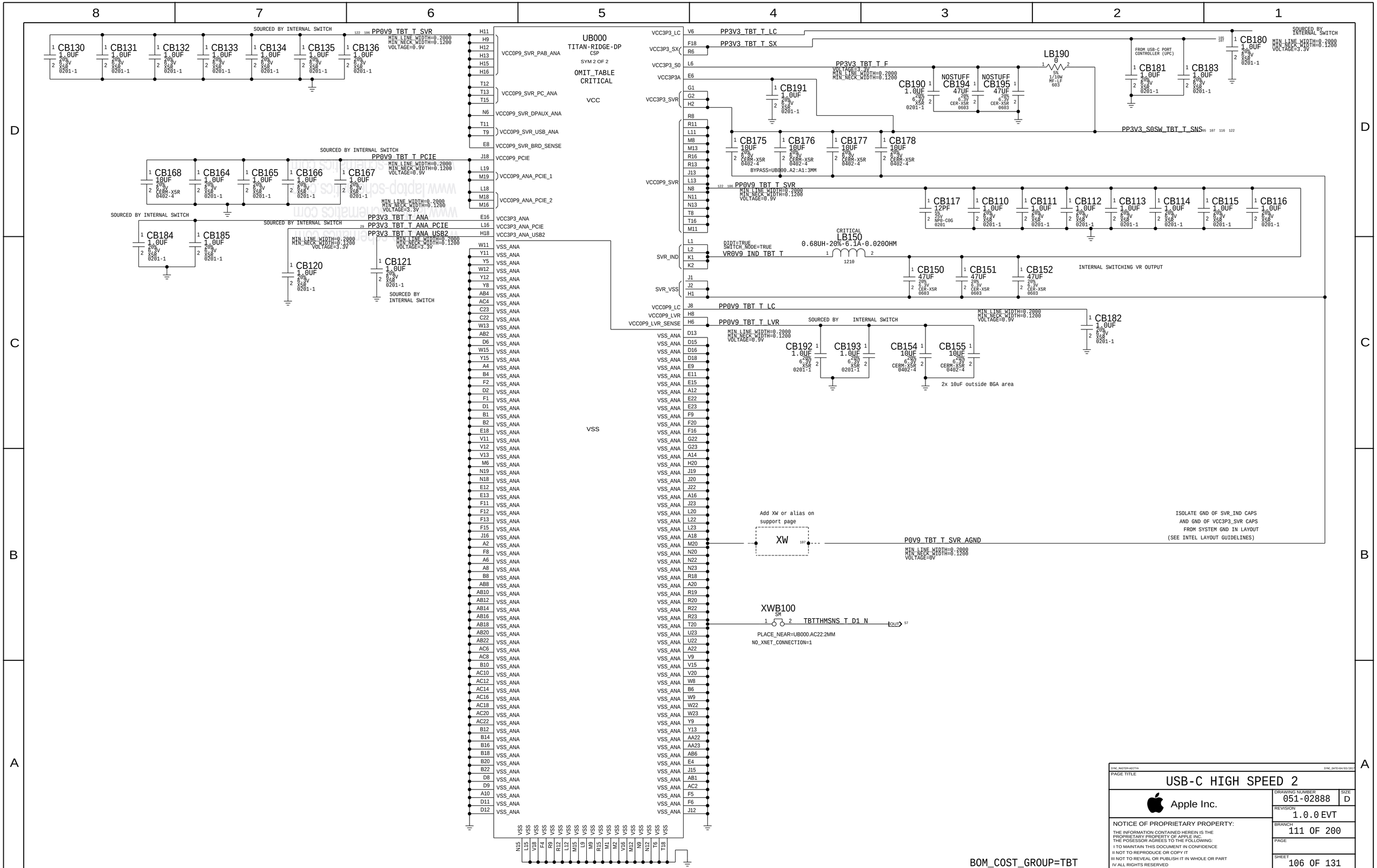


PAGE TITLE
USB-C HIGH SPEED 2

Apple Inc.

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SIZE D
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BRANCH 111 OF 200
PAGE
SHEET 106 OF 131

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## DP SRC OPTIONS
IF DP SRC NOT USED

DP_T_SRC_HPD — RB240 100K 5% 1/20W MF 201

=DP_T_SRC_ML_P<3..0> — NC_DP_T_SRC_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
=DP_T_SRC_ML_N<3..0> — NC_DP_T_SRC_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_T_SRC_AUX_P — NC_DP_T_SRC_AUX_P (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_T_SRC_AUX_N — NC_DP_T_SRC_AUX_N (MAKE_BASE=TRUE, NO_TEST=1)

## FUSES FOR UPC

PLACE_NEAR=QB300:5MM
CRITICAL
FB200 0603
6AMP-32V-0.00950HM
PP20V_USBC_TA_VBUS — PP20V_USBC_TA_VBUS_F

PLACE_NEAR=QB400:5MM
CRITICAL
FB201 0603 740S0135
6AMP-32V-0.00950HM
PP20V_USBC_TB_VBUS — PP20V_USBC_TB_VBUS_F

## 25MHz xtal

TBT_T_XTAL25M_OUT (IN) — CB202 20PF 5% 25V C0G 0201
to/from Ridge
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
TBT_T_XTAL25M_IN (OUT) — CB203 20PF 5% 25V C0G 0201

## USBC 5V EN PD

UPC_T_5V_EN — RB232 100K 5% 1/20W MF 201

## ACE A/B RPD STRAPPING

USBC_TA_CC1 — USBC_TA_CC1 (MAKE_BASE=TRUE)
USBC_TB_CC1 — USBC_TB_CC1 (MAKE_BASE=TRUE)
USBC_TA_CC2 — USBC_TA_CC2 (MAKE_BASE=TRUE)
USBC_TB_CC2 — USBC_TB_CC2 (MAKE_BASE=TRUE)

## I2C SERIES R'S

I2C_UPC_T_SDA2 — RB241 33 5% 1/20W MF 201 — I2C_UPC_SDA (PLACE_NEAR=U3900.J4:5mm)
I2C_UPC_T_SDA2 (MAKE_BASE=TRUE)
I2C_UPC_T_SDA2

I2C_UPC_T_SCL2 — RB242 33 5% 1/20W MF 201 — I2C_UPC_SCL (PLACE_NEAR=U3900.M3:5mm)
I2C_UPC_T_SCL2 (MAKE_BASE=TRUE)
I2C_UPC_T_SCL2

## ACE FET DCIN Bypass Caps

PPDCIN_G3H
CB211 0.10F 10% 35V CER-X5R 0201
CB212 0.10F 10% 35V CER-X5R 0201
CB213 0.10F 10% 35V CER-X5R 0201
CB214 0.10F 10% 35V CER-X5R 0201

PP1V8_SLPS2R
NOSTUFF RB268 47K 5% 1/20W MF 201
NOSTUFF RB267 47K 5% 1/20W MF 201

## ACE PDs

UPC_TA_DBG3 — RB260 100K
UPC_TA_DBG4 — RB261 100K
UPC_TB_DBG3 — RB262 100K
UPC_TB_DBG4 — RB263 100K
NOSTUFF SMC_DEBUGPRT_TX — RB264 100K
NOSTUFF SMC_DEBUGPRT_RX — RB265 100K
TBT_TA_LSTX — RB235 100K
TBT_TA_LSRX — RB236 100K
TBT_TB_LSTX — RB237 100K
TBT_TB_LSRX — RB238 100K
UPC_TB_DBG1 — RB266 100K
UPC_TB_DBG2 — RB239 100K
UPC_TA_GPIO7 — RB243 100K
UPC_TB_GPIO7 — RB249 100K
(5% 1/20W MF 201)

## ACE ARKANOID CONN

Place on bottom
USBC_DBG
JB200 505070-1222 M-ST-SM

| | | | |
|---|---|---|---|
| I2C_TBT_TB_INT_L (CKPLUS_WAIVE=I2C_PULLUP) | 1 | 2 | I2C_TBT_TA_INT_L |
| I2C_UPC_T_SCL2 (CKPLUS_WAIVE=I2C_PULLUP) | 3 | 4 | I2C_TBT_T_SDA |
| I2C_UPC_T_SDA2 | 5 | 6 | I2C_TBT_T_SCL |
| UPC_I2C_INT_L | 7 | 8 | TBT_T_CIO_PWR_EN |
| TBT_T_SPI_CLK_DBG | 9 | 10 | TBT_T_USB_PWR_EN |
| UPC_TA_UART_TX | 11 | 12 | UPC_TA_UART_RX |
| | 13, 14, 15, 16 | | |

## SIGNAL ALIASES

USB2_UPC_TB_P — USB2_UPC_TB_P
USB2_UPC_TB_N — USB2_UPC_TB_N
USB2_UPC_TA_P — USB2_UPC_TA_P
USB2_UPC_TA_N — USB2_UPC_TA_N
(MAKE_BASE=TRUE)

## TBT to ACE

**TBT** — Alpine Ridge U2800 (MASTER)
**Pri ACE** — U3100 (Write: 0x70 Read: 0x71)
**Sec ACE** — U3200 (Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L
(MAKE_BASE=TRUE)

## POWER ALIASES

PP3V3_UPC_TA_LDO — PP3V3_UPC_TA_LDO (MAKE_BASE=TRUE)
PP20V_USBC_TA_VBUS — PP20V_USBC_TA_VBUS (MAKE_BASE=TRUE)
PP20V_USBC_TB_VBUS — PP20V_USBC_TB_VBUS (MAKE_BASE=TRUE)
PP5V_S4_T_USBC — PP5V_S4_T_USBC (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V)
PP3V3_S0SW_TBT_T_SNS — PP3V3_S0SW_TBT_T_SNS (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V)
PP3V3_TBT_T_SX — PP3V3_TBT_T_SX (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)
PP1V8_SLPS2R — PP1V8_SLPS2R

USBC_T_RESET_L — USBC_T_RESET_L (MAKE_BASE=TRUE)
UPC_T_5V_EN — UPC_T_5V_EN (MAKE_BASE=TRUE)
TP_USBC_TB_RESET_L — TP_USBC_TB_RESET_L (MAKE_BASE=TRUE)
TBT_POC_RESET (IN) — TBT_POC_RESET (OUT) (MAKE_BASE=TRUE)
UPC_PMU_RESET — UPC_PMU_RESET (MAKE_BASE=TRUE)
XDP_JTAG_ISP_TDO — XDP_JTAG_ISP_TDO (MAKE_BASE=TRUE)
TBT_T_HDMI_DDC_DATA — TBT_T_HDMI_DDC_DATA (MAKE_BASE=TRUE)
TBT_T_HDMI_DDC_CLK — TBT_T_HDMI_DDC_CLK (MAKE_BASE=TRUE)
JTAG_ISP_TDI — RB256 0 — XDP_JTAG_ISP_TDI
JTAG_ISP_TCK — RB257 0 — XDP_JTAG_ISP_TCK
UPC_TA_FAULT_L (IN) — RB258 0 — XDP_USB_EXTC_OC_L
UPC_TB_FAULT_L (IN) — RB259 0 — XDP_USB_EXTD_OC_L
(5% 1/20W MF 0201)

## AR/ACE SPI BUS SERIES R'S

ROM: TBT_T_SPI_CLK, TBT_T_SPI_CS_L, TBT_T_SPI_MOSI, TBT_T_SPI_MISO

| | | | |
|---|---|---|---|
| RB290 | 100 | TBT_T_SPI_CLK_DBG | |
| RB280 | 15 | UPC_TA_SPI_CLK | Ace |
| RB281 | 15 | UPC_TA_SPI_CS_L | Ace |
| RB282 | 15 | UPC_TA_SPI_MOSI | Ace |
| RB283 | 15 | UPC_TA_SPI_MISO | Ace |
| RB284 | 15 | UPC_T_SPI_CLK | AR |
| RB285 | 15 | UPC_T_SPI_CS_L | AR |
| RB286 | 15 | UPC_T_SPI_MOSI | AR |
| RB287 | 15 | UPC_T_SPI_MISO | AR |

(5% 1/20W MF 201)

## GND ALIASES

GND (MAKE_BASE=TRUE)

## Ridge PCIE Caps

### R2D

| | | |
|---|---|---|
| PCIE_TBT_T_R2D_C_P<0> | CB240 0.22UF | PCIE_TBT_T_R2D_P<0> |
| PCIE_TBT_T_R2D_C_N<0> | CB241 0.22UF | PCIE_TBT_T_R2D_N<0> |
| PCIE_TBT_T_R2D_C_P<1> | CB242 0.22UF | PCIE_TBT_T_R2D_P<1> |
| PCIE_TBT_T_R2D_C_N<1> | CB243 0.22UF | PCIE_TBT_T_R2D_N<1> |
| PCIE_TBT_T_R2D_C_P<2> | CB244 0.22UF | PCIE_TBT_T_R2D_P<2> |
| PCIE_TBT_T_R2D_C_N<2> | CB245 0.22UF | PCIE_TBT_T_R2D_N<2> |
| PCIE_TBT_T_R2D_C_P<3> | CB246 0.22UF | PCIE_TBT_T_R2D_P<3> |
| PCIE_TBT_T_R2D_C_N<3> | CB247 0.22UF | PCIE_TBT_T_R2D_N<3> |

(GND_VOID=TRUE; 0201 X5R 6.3V 20%)

### D2R

| | | |
|---|---|---|
| PCIE_TBT_T_D2R_C_P<0> | CB250 0.22UF | PCIE_TBT_T_D2R_P<0> |
| PCIE_TBT_T_D2R_C_N<0> | CB251 0.22UF | PCIE_TBT_T_D2R_N<0> |
| PCIE_TBT_T_D2R_C_P<1> | CB252 0.22UF | PCIE_TBT_T_D2R_P<1> |
| PCIE_TBT_T_D2R_C_N<1> | CB253 0.22UF | PCIE_TBT_T_D2R_N<1> |
| PCIE_TBT_T_D2R_C_P<2> | CB254 0.22UF | PCIE_TBT_T_D2R_P<2> |
| PCIE_TBT_T_D2R_C_N<2> | CB255 0.22UF | PCIE_TBT_T_D2R_N<2> |
| PCIE_TBT_T_D2R_C_P<3> | CB256 0.22UF | PCIE_TBT_T_D2R_P<3> |
| PCIE_TBT_T_D2R_C_N<3> | CB257 0.22UF | PCIE_TBT_T_D2R_N<3> |

(GND_VOID=TRUE; 0201 X5R 6.3V 20%)

## NO TEST

NC_UPC_TB_I2C_ADDR (IN)

## RIDGE 0.9V SVR XW

P0V9_TBT_T_SVR_AGND — XWB200 SM — NO_XNET_CONNECTION=1

BOM_COST_GROUP=TBT

| | |
|---|---|
| PAGE TITLE | USB-C T Support |
| Apple Inc. | |
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 EVT |
| BRANCH | 112 OF 200 |
| PAGE | |
| SHEET | 107 OF 131 |

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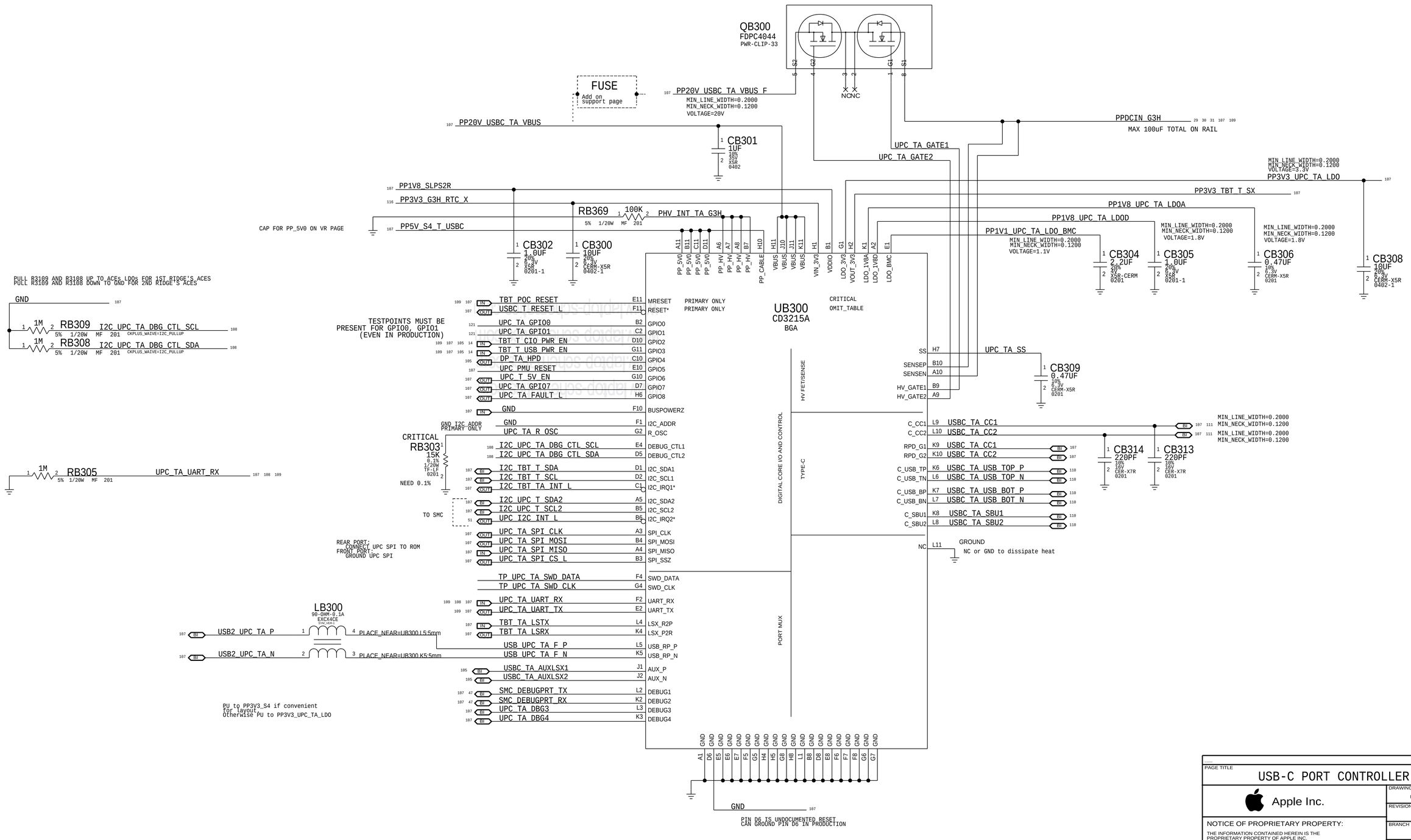
# PRIMARY ACE USB-C PORT CONTROLLER (UPC)




PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0
BRANCH EVT
PAGE 113 OF 200
SHEET 108 OF 131

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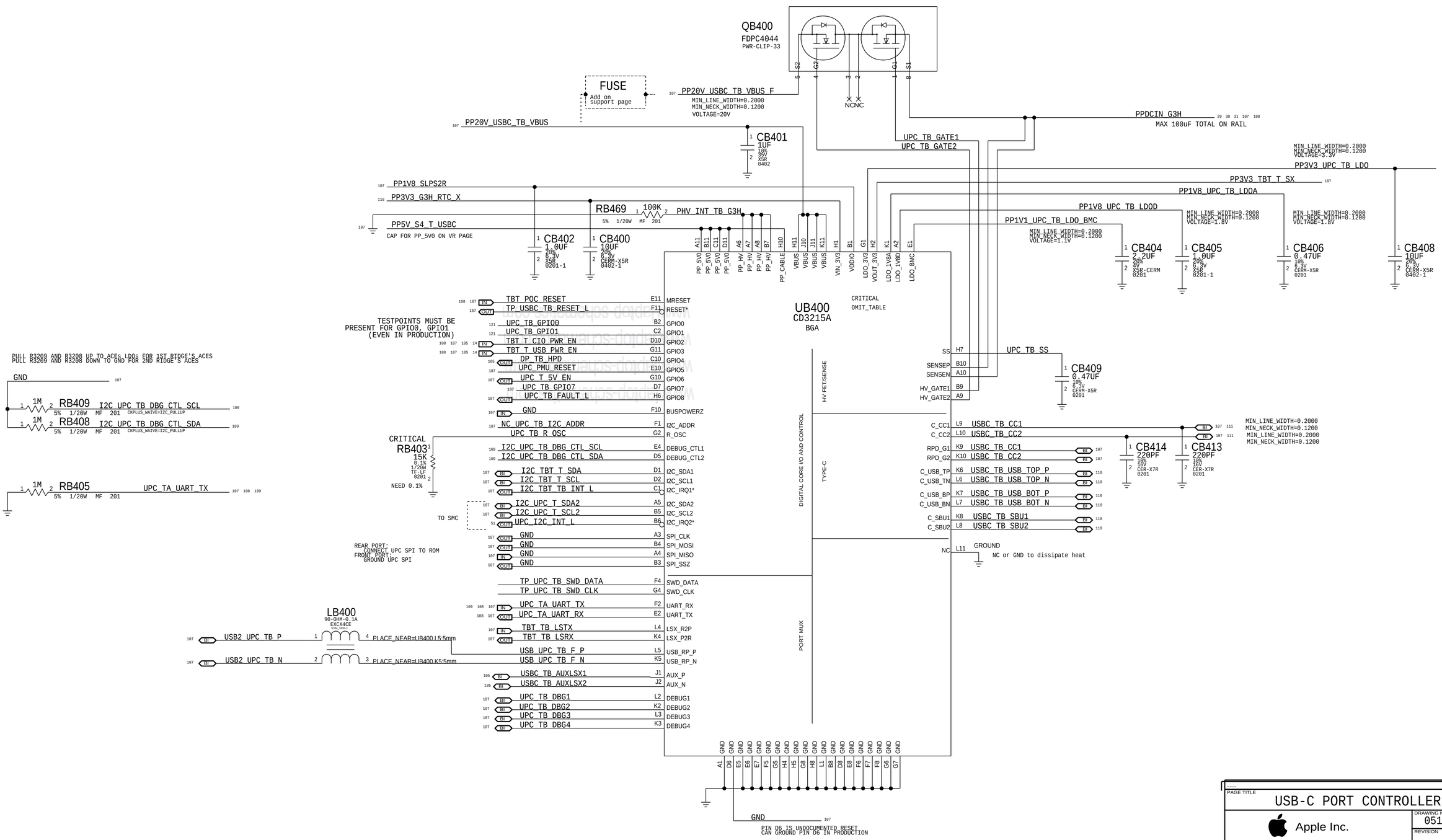
# SECONDARY ACE USB-C PORT CONTROLLER (UPC)

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| Apple Inc. | |
| DRAWING NUMBER | 051-02888 |
| SIZE | D |
| REVISION | 1.0.0 |
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| PAGE | 114 OF 200 |
| SHEET | 109 OF 131 |

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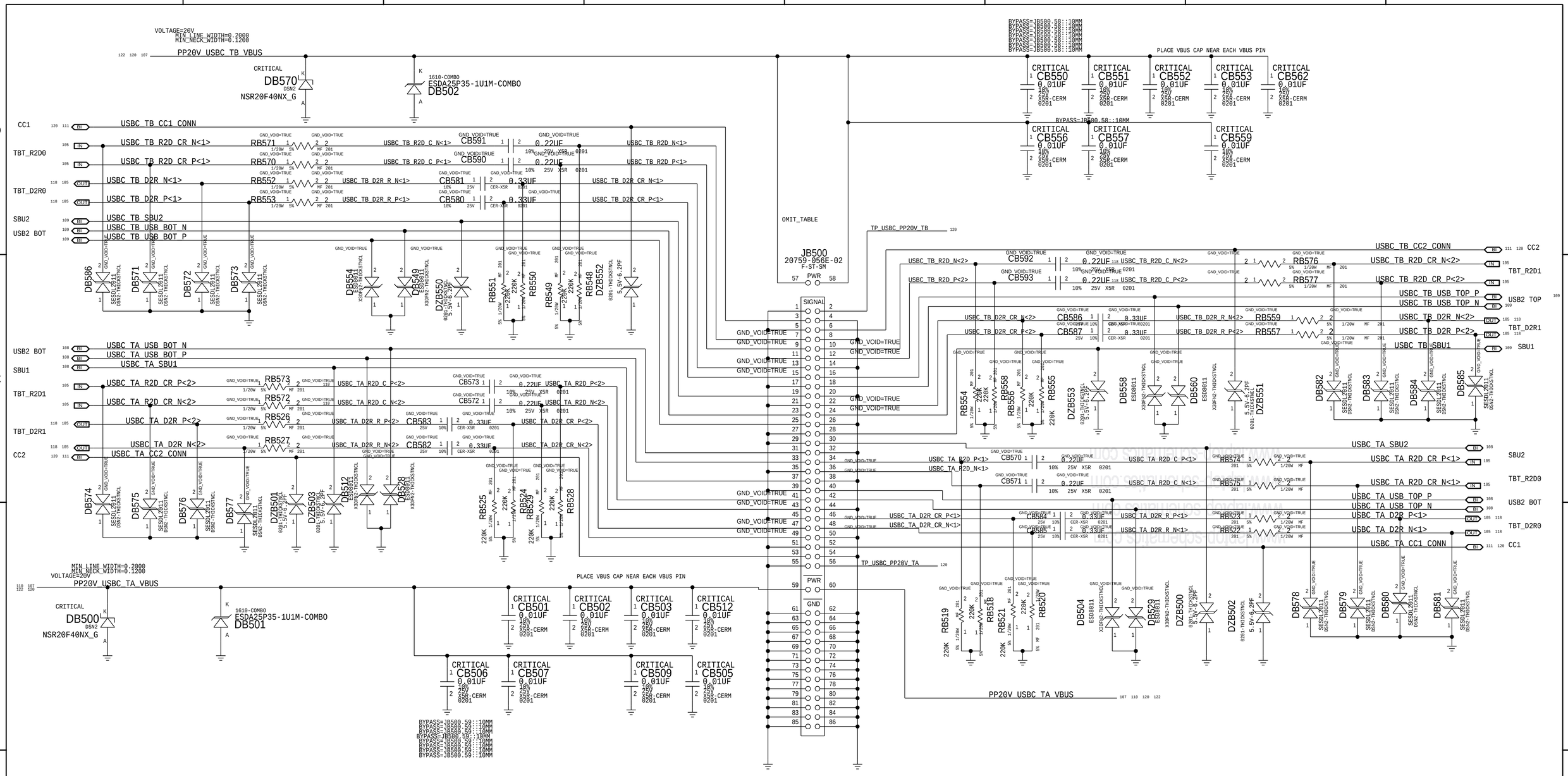


LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 115 OF 200

PAGE

SHEET 110 OF 131

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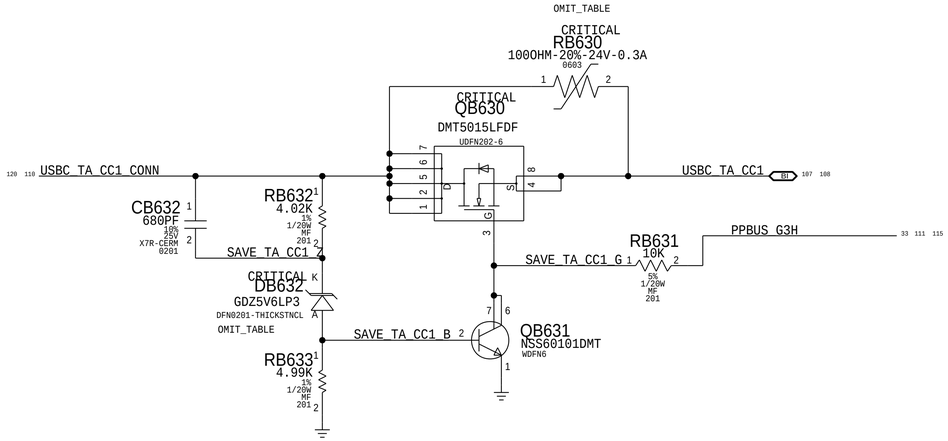
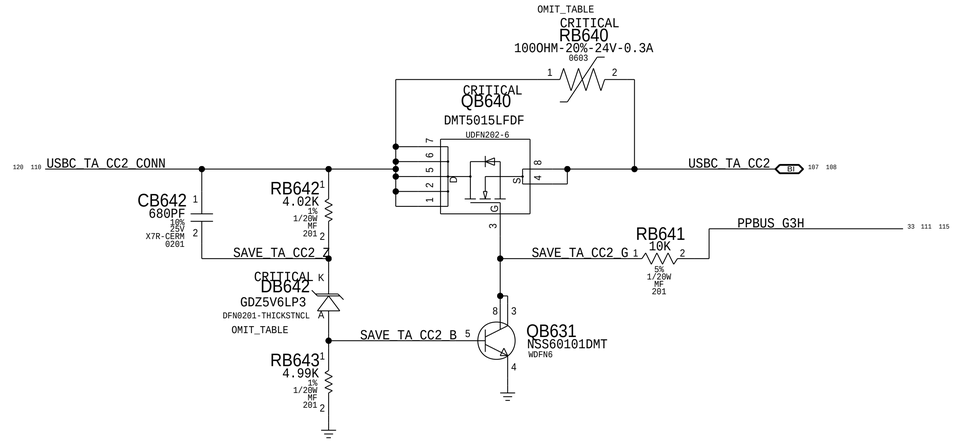
# TA CC Protection

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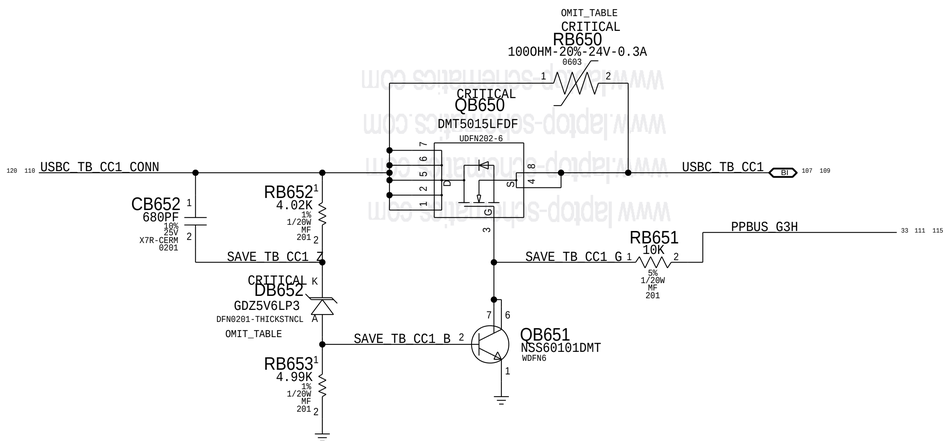


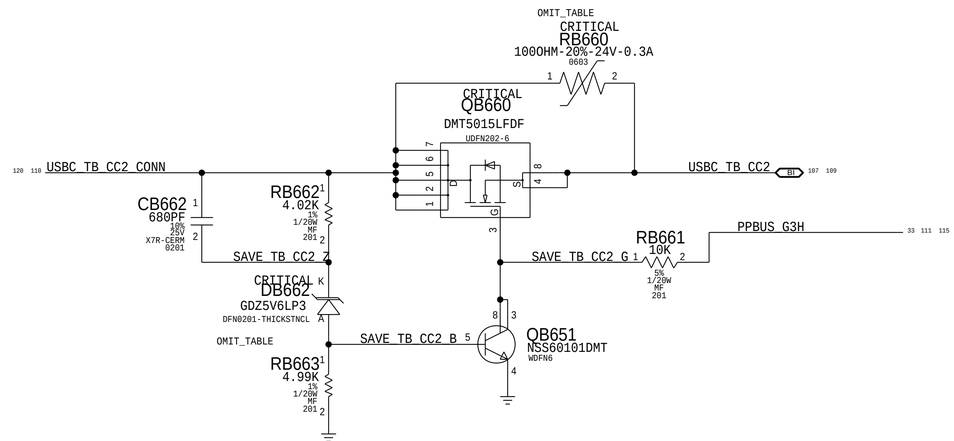


| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 371S00181 | 4 | DIODE,ZENER,5.6V,250MW,DFN0201 | DB632,DB642,DB652,DB662 | CRITICAL | |
| 740S00050 | 4 | FUSE,THRMSTR,PTC,470OHM,24V,60MA,0603 | RB630,RB640,RB650,RB660 | CRITICAL | |

BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC T Connector Support

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0 EVT
BRANCH 116 OF 200
PAGE
SHEET 111 OF 131

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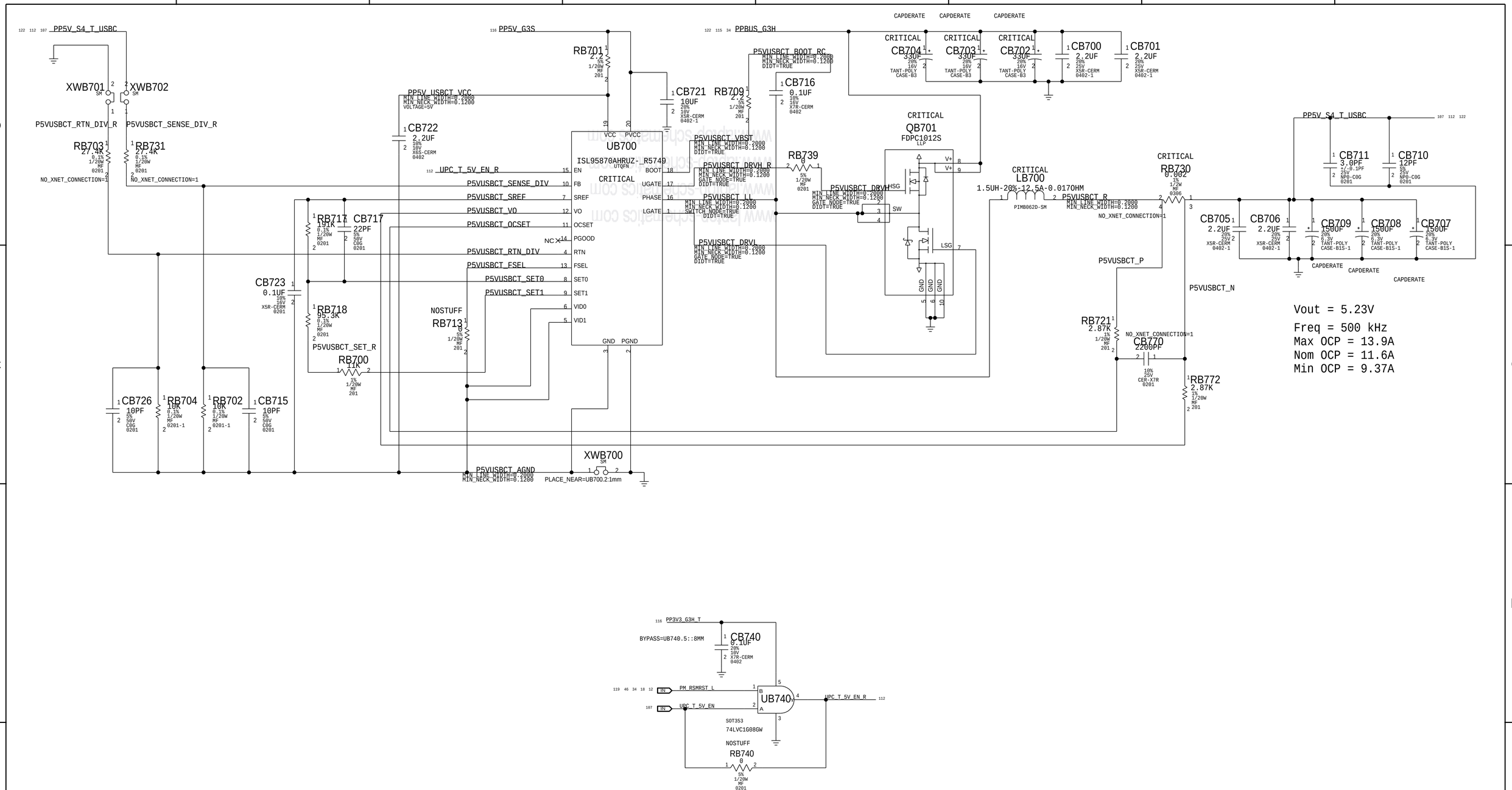


BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C T 5V VR

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DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0 EVT
BRANCH 117 OF 200
PAGE
SHEET 112 OF 131

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BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=j888_copy SYNC_DATE=02/01/2017

PAGE TITLE

GDDR5 VRAM FB 3

Apple Inc.

DRAWING NUMBER 051-02888

SIZE D

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BRANCH 118 OF 200

PAGE

SHEET 113 OF 131

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PAGE TITLE

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BRANCH 119 OF 200

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## PBUS & High Side

122 68 PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 55 119 122 74
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 58
- PPBUS_G3H — 53
- PPBUS_G3H — 34 112 122
- PPBUS_G3H — 65
- PPBUS_G3H — 62 63
- PPBUS_G3H — 33 111
- PPBUS_G3H — 77
- PPBUS_G3H — 55
- PPBUS_G3H — 55
- PPBUS_G3H — 81

53 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 122 124
- PPBUS_HS_CPU — 70
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 72
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 78
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 69

58 PPBUS_HS_GPU
- PPBUS_HS_GPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 101 119 124
- PPBUS_HS_GPU — 98
- PPBUS_HS_GPU — 104
- PPBUS_HS_GPU — 98 101
- PPBUS_HS_GPU — 98

53 PPBUS_HS_OTH5V
- PPBUS_HS_OTH5V — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH5V — 73

53 PPBUS_HS_3V3G3H_T
- PPBUS_HS_3V3G3H_T — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3H_T — 73

53 PPBUS_HS_3V3G3HRTC_X
- PPBUS_HS_3V3G3HRTC_X — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3HRTC_X — 67

## CPU Rails

70 PPVCC_S0_CPU
- PPVCC_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.52V, MAKE_BASE=TRUE — 119
- PPVCC_S0_CPU — 6 8 58
- PPVCC_S0_CPU — 10

71 PPVCCSA_S0_CPU
- PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.52V, MAKE_BASE=TRUE — 119
- PPVCCSA_S0_CPU — 8 58
- PPVCCSA_S0_CPU — 11

72 PPVCCGT_S0_CPU
- PPVCCGT_S0_CPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.52V, MAKE_BASE=TRUE — 119
- PPVCCGT_S0_CPU — 8 58
- PPVCCGT_S0_CPU — 11 122

122 78 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.95V, MAKE_BASE=TRUE — 119
- PPVCCIO_S0_CPU — 5 8 10

## DDR4 1.2V

74 PP1V2_S3
- PP1V2_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 119 122 123
- PP1V2_S3 — 24 25
- PP1V2_S3 — 21
- PP1V2_S3 — 22 23 26
- PP1V2_S3 — 54
- PP1V2_S3 — 79

54 PP1V2_S3_CPUDDR
- PP1V2_S3_CPUDDR — MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.2000, MAKE_BASE=TRUE, VOLTAGE=1.2V — 120
- PP1V2_S3_CPUDDR — 8
- PP1V2_S3_CPUDDR — 10 122

79 PP1V2_S0SW
- PP1V2_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 119
- PP1V2_S0SW — 8

21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

21 PP0V6_S3_MEM_VREFCA_B
- PP0V6_S3_MEM_VREFCA_B — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

## DDR4 0.6V VTT

74 PP0V6_S0_DDRVTT
- PP0V6_S0_DDRVTT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.6V, MAKE_BASE=TRUE — 119
- PP0V6_S0_DDRVTT — 122
- PP0V6_S0_DDRVTT — 122
- PP0V6_S0_DDRVTT — 26
- PP0V6_S0_DDRVTT — 26

## DDR4 2.5V

74 PP2V5_S3
- PP2V5_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=2.5V, MAKE_BASE=TRUE — 119 122 123
- PP2V5_S3 — 22 23
- PP2V5_S3 — 24 25
- PP2V5_S3 — 74

## PMIC Buck 8 - PCH 1.05V Prime

54 PP1V05_PRIM
- PP1V05_PRIM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_PRIM — 16 17 80
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16 17
- PP1V05_PRIM — 17
- PP1V05_PRIM — 18
- PP1V05_PRIM — 74

## PMIC Buck8 SW2

70 PP1V05_S3
- PP1V05_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_S3 — 6 8 11 46
- PP1V05_S3 — 69
- PP1V05_S3 — 8 11
- PP1V05_S3 — 46
- PP1V05_S3 — 77

## PMIC HIO SW

76 PP1V05_S0SW
- PP1V05_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_S0SW — 6 8 11
- PP1V05_S0SW — 18

## GPU Rails

101 98 PPVCORE_S0_GPU
- PPVCORE_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.1V, MAKE_BASE=TRUE — 119 124
- PPVCORE_S0_GPU — 58 96 124

98 PPVDDCI_S0_GPU
- PPVDDCI_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.4V, MAKE_BASE=TRUE — 119
- PPVDDCI_S0_GPU — 58 96 124
- PPVDDCI_S0_GPU — 96

122 98 PP1V5R1V35_S0_GPU_MEM
- PP1V5R1V35_S0_GPU_MEM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.55V, MAKE_BASE=TRUE — 96 119
- PP1V5R1V35_S0_GPU_MEM — 99 100 124
- PP1V5R1V35_S0_GPU_MEM — 58

58 PP1V5R1V35_S0_GPU_IC
- PP1V5R1V35_S0_GPU_IC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.5V, MAKE_BASE=TRUE — 97 124
- PP1V5R1V35_S0_GPU_IC — 96

122 104 PP1V8_GPU
- PP1V8_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_GPU — 58

122 58 PP1V8_S0_GPU
- PP1V8_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 95 103
- PP1V8_S0_GPU — 96
- PP1V8_S0_GPU — 103
- PP1V8_S0_GPU — 102
- PP1V8_S0_GPU — 102
- PP1V8_S0_GPU — 101

104 PP3V3_S0_GPU
- PP3V3_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V, MAKE_BASE=TRUE — 97 103
- PP3V3_S0_GPU — 96
- PP3V3_S0_GPU — 19
- PP3V3_S0_GPU — 95
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 51 103
- PP3V3_S0_GPU — 98 101
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 94

## Digital Ground

GND
- MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000

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REVISION: 1.0.0 EVT
BRANCH: 120 OF 200
PAGE:
SHEET: 115 OF 131

## 1.8V G3S

```
79 PP1V8_G3S
   PP1V8_G3S   MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V MAKE_BASE=TRUE   37 119
   PP1V8_G3S   51
   PP1V8_G3S   66
   PP1V8_G3S   52 61
   PP1V8_G3S   73
   PP1V8_G3S   59 119
   PP1V8_G3S   63
   PP1V8_G3S   62
   PP1V8_G3S   64
   PP1V8_G3S   19
   PP1V8_G3S   54
   PP1V8_G3S   49
   PP1V8_G3S   64
   PP1V8_G3S   52
   PP1V8_G3S   52
   PP1V8_G3S   52
   PP1V8_G3S   52 82
   PP1V8_G3S   48
```

## 5V G3S

```
73 PP5V_G3S
   PP5V_G3S   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V MAKE_BASE=TRUE   119 120
   PP5V_G3S   65
   PP5V_G3S   78 116
   PP5V_G3S   74
   PP5V_G3S   112
   PP5V_G3S   69 70 71
   PP5V_G3S   98 101
   PP5V_G3S   98
   PP5V_G3S   65
   PP5V_G3S   65
   PP5V_G3S   50
   PP5V_G3S   82
   PP5V_G3S   72
   PP5V_G3S   81
   PP5V_G3S   54 56
   PP5V_G3S   51
   PP5V_G3S   78 116
   PP5V_G3S   34
   PP5V_G3S   104
   PP5V_G3S   59
   PP5V_G3S   82
   PP5V_G3S   126
```

## 3V3 G3H "T"

```
73 PP3V3_G3H_T
   PP3V3_G3H_T   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V MAKE_BASE=TRUE   119
   PP3V3_G3H_T   79
   PP3V3_G3H_T   79
   PP3V3_G3H_T   79
   PP3V3_G3H_T   79
   PP3V3_G3H_T   56
   PP3V3_G3H_T   48
   PP3V3_G3H_T   79
   PP3V3_G3H_T   184
   PP3V3_G3H_T   55
   PP3V3_G3H_T   112
```

## 3V3 G3H "X"

```
67 PP3V3_G3H_RTC_X
   PP3V3_G3H_RTC_X   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE   120
   PP3V3_G3H_RTC_X   79
   PP3V3_G3H_RTC_X   184
   PP3V3_G3H_RTC_X   31
   PP3V3_G3H_RTC_X   30
   PP3V3_G3H_RTC_X   126
   PP3V3_G3H_RTC_X   82
   PP3V3_G3H_RTC_X   67
   PP3V3_G3H_RTC_X   67
   PP3V3_G3H_RTC_X   77
   PP3V3_G3H_RTC_X   55
   PP3V3_G3H_RTC_X   79
   PP3V3_G3H_RTC_X   65
   PP3V3_G3H_RTC_X   76
   PP3V3_G3H_RTC_X   79
   PP3V3_G3H_RTC_X   76
   PP3V3_G3H_RTC_X   76
   PP3V3_G3H_RTC_X   29
   PP3V3_G3H_RTC_X   55
   PP3V3_G3H_RTC_X   67
   PP3V3_G3H_RTC_X   126
   PP3V3_G3H_RTC_X   131
   PP3V3_G3H_RTC_X   34
   PP3V3_G3H_RTC_X   108
   PP3V3_G3H_RTC_X   109
```

## 3V3 G3S "T"

```
79 PP3V3_G3S_T
   PP3V3_G3S_T   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_G3S_T   65
   PP3V3_G3S_T   65 120
   PP3V3_G3S_T   66
   PP3V3_G3S_T   49
   PP3V3_G3S_T   61
```

## 3V3 G3S "X"

```
79 PP3V3_G3S_X
   PP3V3_G3S_X   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE   119
   PP3V3_G3S_X   54
   PP3V3_G3S_X   82
```

```
79 PP3V3_S0SW_TBT_X
   PP3V3_S0SW_TBT_X   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE   119
   PP3V3_S0SW_TBT_X   56

79 PP3V3_S0SW_TBT_T
   PP3V3_S0SW_TBT_T   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_S0SW_TBT_T   56

56 PP3V3_S0SW_TBT_X_SNS
   PP3V3_S0SW_TBT_X_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_S0SW_TBT_X_SNS   28 29 95 122
   PP3V3_S0SW_TBT_X_SNS   14

56 PP3V3_S0SW_TBT_T_SNS
   PP3V3_S0SW_TBT_T_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_S0SW_TBT_T_SNS   95 106 107 122
   PP3V3_S0SW_TBT_T_SNS   14

79 PP3V3_G3SSW_SNS
   PP3V3_G3SSW_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_G3SSW_SNS   53
   PP3V3_G3SSW_SNS   53 54 55 56 58
   PP3V3_G3SSW_SNS   54
   PP3V3_G3SSW_SNS   53
   PP3V3_G3SSW_SNS   56

56 PP3V3_G3H_SOCPMU
   PP3V3_G3H_SOCPMU   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE   119
   PP3V3_G3H_SOCPMU   75
   PP3V3_G3H_SOCPMU   76
   PP3V3_G3H_SOCPMU   76

54 PP3V3_G3S_WLAN
   PP3V3_G3S_WLAN   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1000 VOLTAGE=3.3V MAKE_BASE=TRUE   120
   PP3V3_G3S_WLAN   36 37 122
   PP3V3_G3S_WLAN   35

122 75 PPVCCPRIMCORE_PRIM_REG
   PPVCCPRIMCORE_PRIM_REG   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.05V MAKE_BASE=TRUE
   PPVCCPRIMCORE_PRIM_REG   54

54 PP1V8_G3S_WLANBT_VDDIO
   PP1V8_G3S_WLANBT_VDDIO   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V MAKE_BASE=TRUE   120
   PP1V8_G3S_WLANBT_VDDIO   19 35 36 37 122

55 PP3V3_G3H_DFR
   PP3V3_G3H_DFR   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_G3H_DFR   50
```

## SSD 3V3_G3H AND PPBUS_G3H

```
55 PP3V3_G3H_SSD0_SNS
   PP3V3_G3H_SSD0_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE   119
   PP3V3_G3H_SSD0_SNS   87

55 PP3V3_G3H_SSD1_SNS
   PP3V3_G3H_SSD1_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PP3V3_G3H_SSD1_SNS   92

55 PPBUS_G3H_SSD0_SNS
   PPBUS_G3H_SSD0_SNS   MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=13.2V MAKE_BASE=TRUE
   PPBUS_G3H_SSD0_SNS   87

55 PPBUS_G3H_SSD1_SNS
   PPBUS_G3H_SSD1_SNS   MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V MAKE_BASE=TRUE
   PPBUS_G3H_SSD1_SNS   92
```

PAGE TITLE

# Power Alias 2

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REVISION 1.0.0 EVT

BRANCH 121 OF 200

PAGE

SHEET 116 OF 131

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## PEG X16 CPU-GPU

| | | | |
|---|---|---|---|
| PEG_GPU_D2R_P<7..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_P<7..0> (OUT) |
| PEG_GPU_D2R_N<7..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_N<7..0> (OUT) |
| PEG_GPU_R2D_C_P<7..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_P<7..0> (IN) |
| PEG_GPU_R2D_C_N<7..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_N<7..0> (IN) |

## GPU Throttle

| H9M Side (After LS) | | GPU Side |
|---|---|---|
| GFX_SELF_THROTTLE_1V8 | MAKE_BASE=TRUE | = GFX_SELF_THROTTLE_1V8 |
| GFX_THROTTLE_1V8_L | MAKE_BASE=TRUE | = GFX_THROTTLE_1V8_L |

## CPU Display Aliases

| | | | |
|---|---|---|---|
| NC_DDI1_ML_C_P<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI1_ML_C_P<3..0> (IN) |
| NC_DDI1_ML_C_N<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI1_ML_C_N<3..0> (IN) |
| NC_DDI1_AUXCH_C_P | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI1_AUXCH_C_P (IN) |
| NC_DDI1_AUXCH_C_N | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI1_AUXCH_C_N (IN) |
| NC_DDI2_ML_C_P<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI2_ML_C_P<3..0> (IN) |
| NC_DDI2_ML_C_N<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI2_ML_C_N<3..0> (IN) |
| NC_DDI2_AUXCH_C_P | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI2_AUXCH_C_P (IN) |
| NC_DDI2_AUXCH_C_N | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI2_AUXCH_C_N (IN) |
| NC_DDI3_ML_P<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI3_ML_P<3..0> (IN) |
| NC_DDI3_ML_N<3..0> | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI3_ML_N<3..0> (IN) |
| NC_DDI3_AUXCH_P | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI3_AUXCH_P (IN) |
| NC_DDI3_AUXCH_N | MAKE_BASE=TRUE, NO_TEST=1 | = | NC_DDI3_AUXCH_N (IN) |

## Thunderbolt Signals Through PEG

| | | | |
|---|---|---|---|
| PCIE_TBT_X_D2R_P<3..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_P<11..8> (OUT) |
| PCIE_TBT_X_D2R_N<3..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_N<11..8> (OUT) |
| PCIE_TBT_X_R2D_C_P<3..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_P<11..8> (IN) |
| PCIE_TBT_X_R2D_C_N<3..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_N<11..8> (IN) |
| PCIE_TBT_T_D2R_P<3..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_P<15..12> (OUT) |
| PCIE_TBT_T_D2R_N<3..0> (IN) | MAKE_BASE=TRUE | = | =PEG_D2R_N<15..12> (OUT) |
| PCIE_TBT_T_R2D_C_P<3..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_P<15..12> (IN) |
| PCIE_TBT_T_R2D_C_N<3..0> (OUT) | MAKE_BASE=TRUE | = | =PEG_R2D_C_N<15..12> (IN) |

## GPU ALIAS

| | | | |
|---|---|---|---|
| GPU_RESET_L (IN) | MAKE_BASE=TRUE | = | GPU_RESET_L (OUT) |
| EG_PEG_CLK100M_N (IN) | MAKE_BASE=TRUE | = | EG_PEG_CLK100M_N (OUT) |
| EG_PEG_CLK100M_P (IN) | MAKE_BASE=TRUE | = | EG_PEG_CLK100M_P (OUT) |

PAGE TITLE
Signal Alias

Apple Inc.

DRAWING NUMBER 051-02888
SIZE D
REVISION 1.0.0 EVT
BRANCH 122 OF 200
PAGE
SHEET 117 OF 131

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# ICT TESTPOINTS , High Speed NO_TEST

## PEG

| | | |
|---|---|---|
| 117 95 | PEG_GPU_D2R_N<7..0> | NO_TEST=1 |
| 117 95 | PEG_GPU_D2R_P<7..0> | NO_TEST=1 |
| 117 95 | PEG_GPU_R2D_C_N<7..0> | NO_TEST=1 |
| 117 95 | PEG_GPU_R2D_C_P<7..0> | NO_TEST=1 |
| 117 29 | PCIE_TBT_X_D2R_P<3..0> | NO_TEST=1 |
| 117 29 | PCIE_TBT_X_D2R_N<3..0> | NO_TEST=1 |
| 117 29 | PCIE_TBT_X_R2D_C_P<3..0> | NO_TEST=1 |
| 117 29 | PCIE_TBT_X_R2D_C_N<3..0> | NO_TEST=1 |
| 117 107 | PCIE_TBT_T_D2R_P<3..0> | NO_TEST=1 |
| 117 107 | PCIE_TBT_T_D2R_N<3..0> | NO_TEST=1 |
| 107 105 | PCIE_TBT_T_D2R_C_P<3..0> | NO_TEST=1 |
| 107 105 | PCIE_TBT_T_D2R_C_N<3..0> | NO_TEST=1 |
| 29 27 | PCIE_TBT_X_D2R_C_P<3..0> | NO_TEST=1 |
| 29 27 | PCIE_TBT_X_D2R_C_N<3..0> | NO_TEST=1 |
| 29 27 | PCIE_TBT_X_R2D_P<3..0> | NO_TEST=1 |
| 29 27 | PCIE_TBT_X_R2D_N<3..0> | NO_TEST=1 |
| 107 105 | PCIE_TBT_T_R2D_P<3..0> | NO_TEST=1 |
| 107 105 | PCIE_TBT_T_R2D_N<3..0> | NO_TEST=1 |
| 117 107 | PCIE_TBT_T_R2D_C_P<3..0> | NO_TEST=1 |
| 117 107 | PCIE_TBT_T_R2D_C_N<3..0> | NO_TEST=1 |
| 95 | PEG_GPU_D2R_C_N<7..0> | NO_TEST=1 |
| 95 | PEG_GPU_D2R_C_P<7..0> | NO_TEST=1 |
| 95 | PEG_GPU_R2D_N<7..0> | NO_TEST=1 |
| 95 | PEG_GPU_R2D_P<7..0> | NO_TEST=1 |

## CPU/PCH CLK

| | | |
|---|---|---|
| 12 6 | CPU_CLK24M_NSSC_CLK_N | NO_TEST=1 |
| 12 6 | CPU_CLK24M_NSSC_CLK_P | NO_TEST=1 |
| 12 6 | CPU_CLK100M_PCIBCLK_N | NO_TEST=1 |
| 12 6 | CPU_CLK100M_PCIBCLK_P | NO_TEST=1 |
| 12 6 | CPU_CLK100M_BCLK_N | NO_TEST=1 |
| 12 6 | CPU_CLK100M_BCLK_P | NO_TEST=1 |
| 20 18 | NC_ITPXDP_CLK100MN | |
| 20 18 | NC_ITPXDP_CLK100MP | |

## MUX

| | | |
|---|---|---|
| 93 5 | DP_INT_TG_ML_N<3..0> | NO_TEST=1 |
| 93 5 | DP_INT_TG_ML_P<3..0> | NO_TEST=1 |
| 93 5 | DP_INT_TG_AUX_N | NO_TEST=1 |
| 93 5 | DP_INT_TG_AUX_P | NO_TEST=1 |
| 103 93 | DP_INT_EG_ML_N<3..0> | NO_TEST=1 |
| 103 93 | DP_INT_EG_ML_P<3..0> | NO_TEST=1 |
| 103 93 | DP_INT_EG_AUX_N | NO_TEST=1 |
| 103 93 | DP_INT_EG_AUX_P | NO_TEST=1 |

## H9M ESPI

| | | |
|---|---|---|
| 39 20 12 | ESPI_IO<0> | NO_TEST=1 |
| 39 20 12 | ESPI_IO<1> | NO_TEST=1 |
| 39 20 12 | ESPI_IO<2> | NO_TEST=1 |
| 39 20 12 | ESPI_IO<3> | NO_TEST=1 |
| 39 | ESPI_IO_R<0> | NO_TEST=1 |
| 39 | ESPI_IO_R<1> | NO_TEST=1 |
| | ESPI_IO_R<3> | NO_TEST=1 |
| 118 39 | ESPI_IO_R<3> | NO_TEST=1 |

| | | |
|---|---|---|
| 118 29 27 | TBT_X_XTAL25M_OUT | NO_TEST=1 |
| 29 27 | TBT_X_XTAL25M_IN | NO_TEST=1 |
| 107 105 | TBT_T_XTAL25M_OUT | NO_TEST=1 |
| 107 105 | TBT_T_XTAL25M_IN | NO_TEST=1 |
| 103 102 | GPU_CLK_IN | NO_TEST=1 |

## H9M SSD NAND

| | | |
|---|---|---|
| 86 85 84 83 | PCIE_SSD0_R2D_P<3..0> | NO_TEST=1 |
| 86 85 84 83 | PCIE_SSD0_R2D_N<3..0> | NO_TEST=1 |
| 86 85 84 83 41 | PCIE_SSD0_D2R_P<3..0> | NO_TEST=1 |
| 86 85 84 83 41 | PCIE_SSD0_D2R_N<3..0> | NO_TEST=1 |
| 86 85 84 83 41 | PCIE_SSD0_R2D_C_P<3..0> | NO_TEST=1 |
| 86 85 84 83 41 | PCIE_SSD0_R2D_C_N<3..0> | NO_TEST=1 |
| 86 85 84 83 | PCIE_SSD0_D2R_C_P<3..0> | NO_TEST=1 |
| 86 85 84 83 | PCIE_SSD0_D2R_C_N<3..0> | NO_TEST=1 |
| 91 90 89 88 | PCIE_SSD1_R2D_P<3..0> | NO_TEST=1 |
| 91 90 89 88 | PCIE_SSD1_R2D_N<3..0> | NO_TEST=1 |
| 91 90 89 88 41 | PCIE_SSD1_D2R_P<3..0> | NO_TEST=1 |
| 91 90 89 88 41 | PCIE_SSD1_D2R_N<3..0> | NO_TEST=1 |
| 91 90 89 88 41 | PCIE_SSD1_R2D_C_P<3..0> | NO_TEST=1 |
| 91 90 89 88 41 | PCIE_SSD1_R2D_C_N<3..0> | NO_TEST=1 |
| 91 90 89 88 | PCIE_SSD1_D2R_C_P<3..0> | NO_TEST=1 |
| 91 90 89 88 | PCIE_SSD1_D2R_C_N<3..0> | NO_TEST=1 |

## XTAL

| | | |
|---|---|---|
| 118 29 27 | TBT_X_XTAL25M_OUT | NO_TEST=1 |
| 12 | PCH_CLK24M_XTALOUT | NO_TEST=1 |
| 77 | PMU_XTAL1 | NO_TEST=1 |
| 77 | PMU_XTAL2 | NO_TEST=1 |

## BAFFIN FRAME BUFFER

| | | |
|---|---|---|
| 99 97 | FB_A1_CS_L | NO_TEST=1 |
| 99 97 | FB_A0_CKE_L | NO_TEST=1 |
| 99 97 | FB_A1_CKE_L | NO_TEST=1 |
| 99 97 | FB_A0_WE_L | NO_TEST=1 |
| 99 97 | FB_A1_WE_L | NO_TEST=1 |
| 100 97 | FB_B1_CS_L | NO_TEST=1 |
| 100 97 | FB_B0_CKE_L | NO_TEST=1 |
| 100 97 | FB_B1_CKE_L | NO_TEST=1 |
| 118 100 97 | FB_B0_WE_L | NO_TEST=1 |
| 118 100 97 | FB_B0_WE_L | NO_TEST=1 |
| 100 97 | FB_B0_CLK_P | NO_TEST=1 |
| 100 97 | FB_B1_CLK_N | NO_TEST=1 |
| 100 97 | FB_B1_CLK_P | NO_TEST=1 |
| 100 97 | FB_B0_RAS_L | NO_TEST=1 |
| 100 97 | FB_B1_RAS_L | NO_TEST=1 |
| 100 97 | FB_B0_CAS_L | NO_TEST=1 |
| 100 97 | FB_B1_CAS_L | NO_TEST=1 |
| 100 97 | FB_B0_CS_L | NO_TEST=1 |
| 99 97 | FB_A0_DQ<31..0> | NO_TEST=1 |
| 99 97 | FB_A1_DQ<31..0> | NO_TEST=1 |
| 99 97 | FB_A0_A<8..0> | NO_TEST=1 |
| 99 97 | FB_A1_A<8..0> | NO_TEST=1 |
| 99 97 | FB_A0_WCLK_N<1..0> | NO_TEST=1 |
| 99 97 | FB_A0_WCLK_P<1..0> | NO_TEST=1 |
| 99 97 | FB_A1_WCLK_N<1..0> | NO_TEST=1 |
| 99 97 | FB_A1_WCLK_P<1..0> | NO_TEST=1 |
| 99 97 | FB_A0_EDC<3..0> | NO_TEST=1 |
| 99 97 | FB_A1_EDC<3..0> | NO_TEST=1 |
| 99 97 | FB_A0_DBI_L<3..0> | NO_TEST=1 |
| 99 97 | FB_A1_DBI_L<3..0> | NO_TEST=1 |
| 99 97 | FB_A0_ABI_L | NO_TEST=1 |
| 99 97 | FB_A1_ABI_L | NO_TEST=1 |
| 99 97 | FB_A0_CLK_N | NO_TEST=1 |
| 99 97 | FB_A0_CLK_P | NO_TEST=1 |
| 99 97 | FB_A1_CLK_N | NO_TEST=1 |
| 99 97 | FB_A1_CLK_P | NO_TEST=1 |
| 99 97 | FB_A0_RAS_L | NO_TEST=1 |
| 99 97 | FB_A1_RAS_L | NO_TEST=1 |
| 99 97 | FB_A0_CAS_L | NO_TEST=1 |
| 99 97 | FB_A1_CAS_L | NO_TEST=1 |
| 99 97 | FB_A0_CS_L | NO_TEST=1 |
| 100 97 | FB_B0_CLK_N | NO_TEST=1 |
| 100 97 | FB_B0_DQ<31..0> | NO_TEST=1 |
| 100 97 | FB_B1_DQ<31..0> | NO_TEST=1 |
| 100 97 | FB_B0_A<8..0> | NO_TEST=1 |
| 100 97 | FB_B1_A<8..0> | NO_TEST=1 |
| 100 97 | FB_B0_WCLK_N<1..0> | NO_TEST=1 |
| 100 97 | FB_B0_WCLK_P<1..0> | NO_TEST=1 |
| 100 97 | FB_B1_WCLK_N<1..0> | NO_TEST=1 |
| 100 97 | FB_B1_WCLK_P<1..0> | NO_TEST=1 |
| 100 97 | FB_B0_EDC<3..0> | NO_TEST=1 |
| 100 97 | FB_B1_EDC<3..0> | NO_TEST=1 |
| 100 97 | FB_B0_DBI_L<3..0> | NO_TEST=1 |
| 100 97 | FB_B1_DBI_L<3..0> | NO_TEST=1 |
| 100 97 | FB_B0_ABI_L | NO_TEST=1 |
| 100 97 | FB_B1_ABI_L | NO_TEST=1 |

## USB-C X

| | | |
|---|---|---|
| 32 27 | USBC_XB_D2R_N<2..1> | NO_TEST=1 |
| 32 27 | USBC_XB_D2R_P<2..1> | NO_TEST=1 |
| 32 27 | USBC_XA_D2R_P<2..1> | NO_TEST=1 |
| 32 | USBC_XB_R2D_C_P<2..1> | NO_TEST=1 |
| 32 27 | USBC_XA_D2R_N<2..1> | NO_TEST=1 |
| 32 | USBC_XB_R2D_C_N<2..1> | NO_TEST=1 |
| 32 | USBC_XA_R2D_C_P<2..1> | NO_TEST=1 |
| 32 | USBC_XA_R2D_C_N<2..1> | NO_TEST=1 |

## DMI

| | | |
|---|---|---|
| 13 5 | DMI_S2N_P<3..0> | NO_TEST=1 |
| 13 5 | DMI_S2N_N<3..0> | NO_TEST=1 |
| 13 5 | DMI_N2S_P<3..0> | NO_TEST=1 |
| 13 5 | DMI_N2S_N<3..0> | NO_TEST=1 |

## DP - CPU/ACE

| | | |
|---|---|---|
| 103 27 | DP_X_SNK0_ML_C_N<3..0> | NO_TEST=1 |
| 103 27 | DP_X_SNK0_ML_C_P<3..0> | NO_TEST=1 |
| 27 | DP_X_SNK0_ML_N<3..0> | NO_TEST=1 |
| 27 | DP_X_SNK0_ML_P<3..0> | NO_TEST=1 |
| 103 27 | DP_X_SNK1_ML_C_N<3..0> | NO_TEST=1 |
| 103 27 | DP_X_SNK1_ML_C_P<3..0> | NO_TEST=1 |
| 27 | DP_X_SNK1_ML_N<3..0> | NO_TEST=1 |
| 27 | DP_X_SNK1_ML_P<3..0> | NO_TEST=1 |
| 105 103 | DP_T_SNK0_ML_C_N<3..0> | NO_TEST=1 |
| 105 103 | DP_T_SNK0_ML_C_P<3..0> | NO_TEST=1 |
| 105 | DP_T_SNK0_ML_N<3..0> | NO_TEST=1 |
| 105 | DP_T_SNK0_ML_P<3..0> | NO_TEST=1 |
| 105 103 | DP_T_SNK1_ML_C_N<3..0> | NO_TEST=1 |
| 105 103 | DP_T_SNK1_ML_C_P<3..0> | NO_TEST=1 |
| 105 | DP_T_SNK1_ML_N<3..0> | NO_TEST=1 |
| 105 | DP_T_SNK1_ML_P<3..0> | NO_TEST=1 |
| 103 27 | DP_X_SNK0_AUXCH_C_P | NO_TEST=1 |
| 103 27 | DP_X_SNK0_AUXCH_C_N | NO_TEST=1 |
| 105 103 | DP_T_SNK0_AUXCH_C_P | NO_TEST=1 |
| 105 103 | DP_T_SNK0_AUXCH_C_N | NO_TEST=1 |
| 27 | DP_X_SNK0_AUXCH_P | NO_TEST=1 |
| 27 | DP_X_SNK0_AUXCH_N | NO_TEST=1 |
| 105 | DP_T_SNK0_AUXCH_P | |
| 105 | DP_T_SNK0_AUXCH_N | |
| 103 27 | DP_X_SNK1_AUXCH_C_P | NO_TEST=1 |
| 103 27 | DP_X_SNK1_AUXCH_C_N | NO_TEST=1 |
| 105 103 | DP_T_SNK1_AUXCH_C_P | NO_TEST=1 |
| 105 103 | DP_T_SNK1_AUXCH_C_N | NO_TEST=1 |
| 27 | DP_X_SNK1_AUXCH_P | NO_TEST=1 |
| 27 | DP_X_SNK1_AUXCH_N | NO_TEST=1 |
| 105 | DP_T_SNK1_AUXCH_P | |
| 105 | DP_T_SNK1_AUXCH_N | |

## CPU/EDP

## MEM

| | | |
|---|---|---|
| 26 23 22 7 | MEM_A_CLK_P<1..0> | NO_TEST=1 |
| 26 23 22 7 | MEM_A_CLK_N<1..0> | NO_TEST=1 |
| 125 23 22 | MEM_A_DQ<63..0> | NO_TEST=1 |
| 125 25 24 | MEM_B_DQ<63..0> | NO_TEST=1 |
| 125 23 22 | MEM_A_DQS_P<7..0> | NO_TEST=1 |
| 125 23 22 | MEM_A_DQS_N<7..0> | NO_TEST=1 |
| 125 25 24 | MEM_B_DQS_P<7..0> | NO_TEST=1 |
| 125 25 24 | MEM_B_DQS_N<7..0> | NO_TEST=1 |
| 26 25 24 7 | MEM_B_CLK_P<1..0> | NO_TEST=1 |
| 26 25 24 7 | MEM_B_CLK_N<1..0> | NO_TEST=1 |

## WIFI

| | | |
|---|---|---|
| 37 | 50_0_ANT | NO_TEST=1 |
| 37 | 50_1_ANT | NO_TEST=1 |
| 37 | 50_2_ANT | NO_TEST=1 |
| 37 | 50_0_COM | NO_TEST=1 |
| 37 | 50_1_COM | NO_TEST=1 |
| 37 | 50_2_COM | NO_TEST=1 |
| 37 | 50_A_0_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_A_0_MATCH | NO_TEST=1 |
| 37 | 50_G_0_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_G_0_MATCH | NO_TEST=1 |
| 37 | 50_A_1_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_A_1_MATCH | NO_TEST=1 |
| 37 | 50_G_1_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_G_1_MATCH | NO_TEST=1 |
| 37 | 50_A_2_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_A_2_MATCH | NO_TEST=1 |
| 37 | 50_G_2_DIPLEXER | NO_TEST=1 |
| 37 36 | 50_G_2_MATCH | NO_TEST=1 |

## USB-C T

| | | |
|---|---|---|
| 110 105 | USBC_TA_D2R_P<2..1> | NO_TEST=1 |
| 110 105 | USBC_TA_D2R_N<2..1> | NO_TEST=1 |
| 110 | USBC_TA_R2D_C_P<2..1> | NO_TEST=1 |
| 110 | USBC_TA_R2D_C_N<2..1> | NO_TEST=1 |
| 110 105 | USBC_TB_D2R_P<2..1> | NO_TEST=1 |
| 110 105 | USBC_TB_D2R_N<2..1> | NO_TEST=1 |
| 110 | USBC_TB_R2D_C_P<2..1> | NO_TEST=1 |
| 110 | USBC_TB_R2D_C_N<2..1> | NO_TEST=1 |

## PCH/AR

| | | |
|---|---|---|
| 36 14 | PCH_PCIE_WLAN_D2R_N | NO_TEST=1 |
| 36 14 | PCH_PCIE_WLAN_D2R_P | NO_TEST=1 |
| 36 14 | PCH_PCIE_WLAN_R2D_C_N | NO_TEST=1 |
| 36 14 | PCH_PCIE_WLAN_R2D_C_P | NO_TEST=1 |
| 36 | PCH_PCIE_WLAN_D2R_C_P | NO_TEST=1 |
| 36 | PCH_PCIE_WLAN_D2R_C_N | NO_TEST=1 |
| 36 | PCH_PCIE_WLAN_R2D_P | NO_TEST=1 |
| 36 | PCH_PCIE_WLAN_R2D_N | NO_TEST=1 |

## PCH/SOC

| | | |
|---|---|---|
| 47 41 | PCIE_SOC_R2D_P<3..0> | NO_TEST=1 |
| 47 41 | PCIE_SOC_R2D_N<3..0> | NO_TEST=1 |
| 41 14 | PCIE_SOC_D2R_P<3..0> | NO_TEST=1 |
| 41 14 | PCIE_SOC_D2R_N<3..0> | NO_TEST=1 |
| 47 14 | PCIE_SOC_R2D_C_P<3..0> | NO_TEST=1 |
| 47 14 | PCIE_SOC_R2D_C_N<3..0> | NO_TEST=1 |
| 41 | PCIE_SOC_D2R_C_P<3..0> | NO_TEST=1 |
| 41 | PCIE_SOC_D2R_C_N<3..0> | NO_TEST=1 |

PAGE TITLE
High speed No Testpoints

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0 EVT
BRANCH 123 OF 200
PAGE
SHEET 118 OF 131

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DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

## DFU TEST POINTS <RDAR://31619312>

Possibly useful panda signals

| | | | |
|---|---|---|---|
| TPC4H8 | TP-P5 | SOC_DEBUGPRT_RX | 40 126 |
| TPC4H9 | TP-P5 | SOC_DEBUGPRT_TX | 40 126 |
| TPC402 | TP-P5 | DEBUG_JTAG_SOC_TDO | 39 126 |
| TPC403 | TP-P5 | DEBUG_JTAG_SOC_TDI | 39 126 |
| TPC404 | TP-P5 | PP1V8_SLPS2R | 80 |
| TPC405 | TP-P5 | SOC_SOCHOT_L | 38 77 126 |
| TPC406 | TP-P5 | I2C_PWR_SDA | 39 51 |
| TPC407 | TP-P5 | I2C_UPC_SCL | 39 51 |
| TPC4E9 | TP-P5 | I2C_UPC_SDA | 39 51 |
| TPC4Z5 | TP-P5 | I2C_PWR_SCL | 39 51 |

## PSU Power input

| | | | |
|---|---|---|---|
| TPC441 | TP-P5 | PPBUS_HS_GPU | 101 115 124 |
| TPC442 | TP-P5 | PP2V5_S3 | 115 122 123 |
| TPC443 | TP-P5 | PP0V6_S0_DDRVTT | 115 119 |
| TPC444 | TP-P5 | PP3V3_S5 | 80 |
| TPC4Z6 | TP-P5 | PPVBAT_G3H_CHGR_REG | 68 |
| TPC4Z7 | TP-P5 | PPDCIN_G3H_CHGR | 68 122 |
| TPC448 | TP-P5 | | |
| TPC449 | TP-P5 | | |
| TPC450 | TP-P5 | | |

## DFU NON-CUSTOMER-FACING USB PORTS

PLACE IN ACCESSIBLE BOARD AREA

SWDL

| | | | |
|---|---|---|---|
| TPC408 | TP-P5 | USB3_TEST_D2R_N | OUT 14 |
| TPC409 | TP-P5 | USB3_TEST_D2R_P | OUT 14 |
| TPC410 | TP-P5 | USB3_TEST_R2D_N | IN 14 |
| TPC411 | TP-P5 | USB3_TEST_R2D_P | IN 14 |
| TPC412 | TP-P5 | | |
| TPC413 | TP-P5 | | |
| TPC414 | TP-P5 | | |
| TPC415 | TP-P5 | | |
| TPC416 | TP-P5 | USB2_UPC_TA_N | BI 14 107 |
| TPC417 | TP-P5 | USB2_UPC_TA_P | BI 14 107 |
| TPC418 | TP-P5 | | |

DZC400, DZC401, DZC402, DZC403: 5.5V-0.28PF 0201-THICKSTNCL

DZC408, DZC409: 5.5V-0.28PF 0201-THICKSTNCL

## NON-CUSTOMER-FACING USB PORTS FOR ETHERNET DONGLE(Bristol OS Testing)

PLACE IN ACCESSIBLE BOARD AREA

Ethenet

| | | | |
|---|---|---|---|
| TPC422 | TP-P5 | USB3_TEST2_D2R_N | OUT 14 |
| TPC423 | TP-P5 | USB3_TEST2_D2R_P | OUT 14 |
| TPC424 | TP-P5 | USB3_TEST2_R2D_N | IN 14 |
| TPC425 | TP-P5 | USB3_TEST2_R2D_P | IN 14 |
| TPC426 | TP-P5 | | |
| TPC427 | TP-P5 | | |
| TPC428 | TP-P5 | | |
| TPC429 | TP-P5 | | |
| TPC419 | TP-P5 | USB2_UPC_TB_N | BI 14 107 |
| TPC420 | TP-P5 | USB2_UPC_TB_P | BI 14 107 |
| TPC421 | TP-P5 | | |
| TPC430 | TP-P5 | PP5V_G3S | 116 119 120 |

DZC410, DZC411, DZC412, DZC413: 5.5V-0.28PF 0201-THICKSTNCL

DZC406, DZC407: 5.5V-0.28PF 0201-THICKSTNCL

## Battery

| | | | |
|---|---|---|---|
| TPC431 | 1 TP-P5 | SYS_DETECT_L | 67 |
| TPC432 | 1 TP-P5 | SMBUS_3V3_BATT_SCL | 67 |
| TPC433 | 1 TP-P5 | SMBUS_3V3_BATT_SDA | 67 |
| TPC434 | 1 TP-P5 | TP_BMON_IOUT | 67 |
| TPC435 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC436 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC437 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC4D5 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC4D6 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC4D7 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC4I7 | 1 TP-P5 | PPVBAT_G3H_CONN | 67 68 119 |
| TPC4Z8 | TP-P5 | SYS_DETECT | 67 |
| TPC4D8 | 1 TP-P5 | | |
| TPC4D9 | 1 TP-P5 | | |
| TPC4E0 | 1 TP-P5 | | |
| TPC4E1 | 1 TP-P5 | | |
| TPC4E2 | 1 TP-P5 | | |
| TPC440 | 1 TP-P5 | | |
| TPC4I6 | 1 TP-P5 | | |

## AUDIO JACK

| | | | |
|---|---|---|---|
| 120 64 | IN | AUD_CONN_HP_LEFT | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_HP_RIGHT | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_RING2 | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_SLEEVE | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_HP_SENSE_L | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_HP_SENSE_R | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_TIP_SENSE | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_SLEEVE_XW | FUNC_TEST=TRUE |
| 120 64 | IN | AUD_CONN_RING2_XW | FUNC_TEST=TRUE |
| | | GND | X2 |
| TPC4Z9 | TP-P5 | GND_AUDIO_CODEC | 61 122 |

## FAN

| | | | |
|---|---|---|---|
| TPC4N0 | 1 TP-P5 | SMC_FAN_0_PWM | 39 59 |
| TPC4N1 | 1 TP-P5 | SMC_FAN_0_TACH | 39 59 |
| TPC4N2 | 1 TP-P5 | SMC_FAN_1_PWM | 39 59 |
| TPC4N3 | 1 TP-P5 | SMC_FAN_1_TACH | 39 59 |
| TPC4N4 | 1 TP-P5 | PP1V8_G3S | 59 116 119 |
| TPC4N5 | 1 TP-P5 | PP1V8_G3S | 59 116 119 |
| TPC4N6 | 1 TP-P5 | | |
| TPC4N7 | 1 TP-P5 | | |

## DEBUG MOJO

| | | | |
|---|---|---|---|
| TPC451 | 1 TP-P5 | PCH_UART_DEBUG_R2D | 15 29 126 |
| TPC452 | 1 TP-P5 | PCH_UART_DEBUG_D2R | 15 29 126 |
| TPC4F1 | 1 TP-P5 | SMC_DEBUGPRT_TX | 39 47 126 |
| TPC4F2 | 1 TP-P5 | SMC_DEBUGPRT_RX | 39 47 126 |
| TPC453 | 1 TP-P5 | | |

## Soc Access w/o Potassium

| | | | |
|---|---|---|---|
| TPC454 | 1 TP-P5 | SOC_USB_VBUS | 29 38 126 |
| TPC455 | 1 TP-P5 | USB_SOC_TYPEC_P | 29 126 |
| TPC456 | 1 TP-P5 | USB_SOC_TYPEC_N | 29 126 |
| TPC457 | 1 TP-P5 | PMU_ACTIVE_READY | 30 38 77 131 |
| TPC458 | 1 TP-P5 | SOC_FORCE_DFU | 29 38 77 131 |
| TPC459 | 1 TP-P5 | SOC_DFU_STATUS | 29 38 131 |
| TPC460 | 1 TP-P5 | UPC_XB_DBG3 | 29 31 |
| TPC461 | 1 TP-P5 | UPC_XB_DBG4 | 29 31 |
| TPC462 | 1 TP-P5 | SOC_DOCK_CONNECT | 30 31 39 |
| TPC464 | 1 TP-P5 | | |

## Power Sequence,status,charging

| | | | |
|---|---|---|---|
| TPC466 | TP-P5 | PP3V3_G3H_SOCPMU | 116 119 |
| TPC468 | TP-P5 | PPBUS_G3H | 55 115 |
| TPC469 | TP-P5 | PP1V2_S3 | 115 122 123 |
| TPC470 | TP-P5 | PPVCC_S0_CPU | 115 |
| TPC471 | TP-P5 | PP5V_G3S | 120 |
| TPC472 | TP-P5 | PP1V5R1V35_S0_GPU_MEM | 96 115 |
| TPC473 | TP-P5 | PPVCORE_S0_GPU | 115 124 |
| TPC4L6 | TP-P5 | CPU_PWRGD | 6 13 121 |
| TPC474 | TP-P5 | PMU_ONOFF_R_L | 48 |
| TPC475 | TP-P5 | PM_SLP_S3_L | 12 14 27 105 131 |
| TPC476 | TP-P5 | PM_SLP_S4_L | 12 |
| TPC477 | TP-P5 | PM_SLP_S5_L | 12 |
| TPC479 | TP-P5 | PP0V6_S0_DDRVTT | 115 119 |
| TPC481 | TP-P5 | PP1V05_S3 | 115 |
| TPC482 | TP-P5 | PM_SYSRST_L | 12 18 46 121 |
| TPC483 | TP-P5 | PM_PCH_SYS_PWROK | 12 46 |
| TPC484 | TP-P5 | PM_PCH_PWROK | 12 35 46 121 |
| TPC485 | TP-P5 | PLT_RST_L | 12 20 46 |
| TPC486 | TP-P5 | PM_RSMRST_L | 12 18 34 46 122 |
| TPC487 | TP-P5 | PM_SLP_S0_L | 12 39 77 131 |
| TPC488 | TP-P5 | SMC_FIXTURE_MODE_L | 39 47 |
| TPC489 | TP-P5 | PP1V8_G3S | 37 116 |
| TPC490 | TP-P5 | PP5V_G3S | 116 119 120 |
| TPC491 | TP-P5 | PP3V3_G3H_T | 116 |
| TPC492 | TP-P5 | PP3V3_G3H_SSD0_SNS | 116 |
| TPC493 | TP-P5 | PP3V3_S0SW_TBT_X | 116 |
| TPC495 | TP-P5 | PP3V3_G3H_SOCPMU | 116 119 |
| TPC4B4 | TP-P5 | PPVDDCPU_AWAKE | 80 |
| TPC4B6 | 1 TP-P5 | PVDDQ_EN_R | 74 |
| TPC4B7 | 1 TP-P5 | PVCCIO_EN | 77 78 |
| TPC4B8 | 1 TP-P5 | PP0V9_SLPDDR | 80 |
| TPC4B9 | 1 TP-P5 | PP1V1_SLPDDR | 80 |
| TPC4C0 | 1 TP-P5 | PP1V1_SLPS2R | 80 |
| TPC4C1 | 1 TP-P5 | PP1V8_AWAKE | 80 |
| TPC4J1 | 1 TP-P5 | SMC_SYSRST_L | 39 46 121 |
| TPC4C4 | 1 TP-P5 | PP1V8_SLPS2R_PMUVDDGPIO | 75 |
| TPC4C5 | 1 TP-P5 | P1V1_SLPDDR_SOCFET_EN | 76 77 131 |
| TPC4C6 | 1 TP-P5 | PMU_CLK32K_WLANBT | 36 77 |
| TPC4C7 | 1 TP-P5 | SOC_WDOG | 39 77 |
| TPC4C8 | 1 TP-P5 | PMU_CLK32K_SOC | 39 77 |
| TPC4C9 | 1 TP-P5 | PMU_SYS_ALIVE | 38 39 77 87 92 93 |
| TPC496 | TP-P5 | | |

BOM_COST_GROUP=DEBUG

## Power Sequence,status,charging

| | | | |
|---|---|---|---|
| TPC4D0 | 1 TP-P5 | P5VG3S_EN | 73 77 |
| TPC4D1 | 1 TP-P5 | PP0V8_SLPS2R | 80 |
| TPC4D2 | 1 TP-P5 | PPVDDCPUSRAM_AWAKE | 80 |
| TPC4D3 | 1 TP-P5 | P5VG3S_PGOOD | 73 77 |
| TPC4D4 | 1 TP-P5 | CPUVR_PGOOD | 77 80 |
| TPC4L7 | TP-P5 | PPVCCGT_S0_CPU | 115 |
| TPC4F3 | TP-P5 | PPVCCSA_S0_CPU | 115 |
| TPC4L0 | TP-P5 | PPVCCIO_S0_CPU | 115 |
| TPC4F4 | TP-P5 | PP1V05_S0SW | 115 |
| TPC4F5 | TP-P5 | PP1V2_S0SW | 115 |
| TPC4F6 | TP-P5 | PP1V05_PRIM | 115 |
| TPC4F7 | TP-P5 | PP1V8_S5 | 80 |
| TPC4F8 | TP-P5 | PP3V0_G3H_RTC | 80 |
| TPC4F9 | TP-P5 | ALL_SYS_PWRGD | 46 77 |
| TPC4G0 | TP-P5 | PCH_RTC_RESET_L | 12 77 |
| TPC4G1 | TP-P5 | PM_THRMTRIP_L | 6 46 |
| TPC4G2 | TP-P5 | PM_PWRBTN_L | 18 80 |
| TPC4G3 | TP-P5 | CPU_PROCHOT_R_L | 6 |
| TPC4G4 | TP-P5 | PPVDDCI_S0_GPU | 115 |
| TPC4G5 | TP-P5 | DISP_GCON_RESET_L | 93 |
| TPC4G6 | TP-P5 | GPU_RESET_L | 46 95 117 |
| TPC4G7 | TP-P5 | PM_MEMVTT_EN | 5 74 |
| TPC4G8 | TP-P5 | ESPI_RESET_L | 12 20 39 |
| TPC4G9 | TP-P5 | GFX_THROTTLE_L | 103 |
| TPC4H0 | TP-P5 | PMU_COLD_RESET_L | 39 64 77 121 |
| TPC4H1 | TP-P5 | PP0V82_SLPDDR | 80 |
| TPC4H2 | TP-P5 | CHGR_EN_MVR | 67 68 |
| TPC4H3 | TP-P5 | PMU_PVDDMAIN_EN | 73 77 |
| TPC4H4 | TP-P5 | UPC_PMU_RESET | 18 67 77 107 |
| TPC4H5 | TP-P5 | P3V3G3S_EN | 77 79 |
| TPC4H6 | TP-P5 | PP3V3_G3S_X | 116 |
| TPC4H7 | TP-P5 | P1V8G3S_EN | 77 79 131 |
| TPC4L1 | TP-P5 | SSD_PMU_RESET_L | 39 47 87 92 |
| TPC4L2 | TP-P5 | PP2V5_NAND_SSD0 | 83 84 85 86 87 124 |
| TPC4I0 | TP-P5 | PP2V5_NAND_SSD1 | 88 89 90 91 92 124 |
| TPC4I1 | TP-P5 | PP0V9_SSD0 | 83 84 85 86 87 124 |
| TPC4I2 | TP-P5 | PP0V9_SSD1 | 88 89 90 91 92 124 |
| TPC4I3 | TP-P5 | PP1V8_SSD1 | 88 89 90 91 92 124 |
| TPC4I4 | TP-P5 | PP1V8_SSD0 | 83 84 85 86 87 124 |
| TPC4I5 | TP-P5 | PP1V2_AWAKE | 80 |

## Soc Access with Potassium

| | | | |
|---|---|---|---|
| TPC499 | 1 TP-P5 | USBC_XB_SBU1 | 31 32 |
| TPC4A0 | 1 TP-P5 | USBC_XB_SBU2 | 31 32 |
| TPC4A1 | 1 TP-P5 | USBC_XA_CC1_CONN | 32 33 |
| TPC4A2 | 1 TP-P5 | PP20V_USBC_XA_VBUS | 29 32 120 122 |
| TPC4A3 | 1 TP-P5 | | |

Left Side - Top Layer

| | | | |
|---|---|---|---|
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4AB |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4AA |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4A5 |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4A6 |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4A7 |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4A8 |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4E5 |
| 119 68 55 53 29 122 | PPDCIN_G3H | 1 TP-P5 | TPC4E6 |
| | | 1 TP-P5 | TPC4A9 |
| | | 1 TP-P5 | TPC4B0 |
| | | 1 TP-P5 | TPC4B1 |
| | | 1 TP-P5 | TPC4B2 |
| | | 1 TP-P5 | TPC4B3 |
| | | 1 TP-P5 | TPC4E7 |
| | | 1 TP-P5 | TPC4E8 |

PAGE TITLE

# DFU TEST POINTS

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 124 OF 200

PAGE

SHEET 119 OF 131

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# FCT TEST POINTS (TOP SIDE OF MLB)

## DFR/MESA (FCT)

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC500 | A / 1 | TP-P5 | | |
| TPC501 | A / 1 | TP-P5 | | |
| TPC502 | A / 1 | TP-P5 | MIPI_DFR_CLK_CONN_FILT_P | 50 |
| TPC503 | A / 1 | TP-P5 | DFR_DISP_VSYNC | 50 |
| TPC505 | A / 1 | TP-P5 | DFR_DISP_TE | 40 50 |
| TPC504 | A / 1 | TP-P5 | MIPI_DFR_CLK_CONN_FILT_N | 50 |
| TPC506 | A / 1 | TP-P5 | | |
| TPC507 | A / 1 | TP-P5 | MIPI_DFR_DATA_CONN_FILT_P | 50 |
| TPC524 | A / 1 | TP-P5 | MIPI_DFR_DATA_CONN_FILT_N | 50 |
| TPC510 | A / 1 | TP-P5 | DFR_DISP_RESET_L | 40 50 |
| TPC516 | A / 1 | TP-P5 | PP3V3_G3HSW_DFR | 50 120 |
| TPC508 | A / 1 | TP-P5 | DFR_DISP_INT | 38 50 |
| TPC518 | A / 1 | TP-P5 | PP3V3_G3HSW_DFR | 50 120 |
| TPC511 | A / 1 | TP-P5 | | |
| TPC512 | A / 1 | TP-P5 | | |
| TPC521 | A / 1 | TP-P5 | TP_DFR_TOUCH_PANEL_DETECT | 50 |
| TPC522 | A / 1 | TP-P5 | DFR_LID_OPEN_L | 50 |
| TPC515 | A / 1 | TP-P5 | | |
| TPC520 | A / 1 | TP-P5 | | |
| TPC527 | A / 1 | TP-P5 | SPI_DFR_MISO_R | 47 50 |
| TPC528 | A / 1 | TP-P5 | SPI_DFR_CS_L | 40 50 |
| TPC533 | A / 1 | TP-P5 | DFR_TOUCH_INT_L | 39 50 |
| TPC535 | A / 1 | TP-P5 | DFR_TOUCH_CLK32K_RESET_L | 40 50 |
| TPC534 | A / 1 | TP-P5 | I2C_DFR_SCL_R | 50 52 |
| TPC536 | A / 1 | TP-P5 | I2C_DFR_SDA_R | 50 52 |
| TPC538 | A / 1 | TP-P5 | DFR_TOUCH_RESET_L | 40 50 |
| TPC530 | A / 1 | TP-P5 | SPI_DFR_MOSI | 47 50 |
| TPC525 | A / 1 | TP-P5 | | |
| TPC526 | A / 1 | TP-P5 | | |
| TPC529 | A / 1 | TP-P5 | SPI_DFR_CLK | 47 50 |
| TPC539 | A / 1 | TP-P5 | TP_DFR_TOUCH_ROM_WC | 50 |
| TPC540 | A / 1 | TP-P5 | PP1V8_SLPS2RSW_DFR | 50 52 120 |
| TPC542 | A / 1 | TP-P5 | PP5V_G3S_DFR_FILT | 50 |
| TPC541 | A / 1 | TP-P5 | PP1V8_SLPS2RSW_DFR | 50 52 120 |
| TPC544 | A / 1 | TP-P5 | SPI_MESA_MISO_CONN | 48 |
| TPC543 | A / 1 | TP-P5 | PP1V8_MESA_CONN | 48 |
| TPC550 | A / 1 | TP-P5 | SPI_MESA_CLK_CONN | 48 |
| TPC531 | A / 1 | TP-P5 | | |
| TPC532 | A / 1 | TP-P5 | | |
| TPC546 | A / 1 | TP-P5 | MESA_INT_CONN | 48 |
| TPC547 | A / 1 | TP-P5 | SPI_MESA_MOSI_CONN | 48 |
| TPC548 | A / 1 | TP-P5 | MESA_BOOST_EN_CONN | 48 |
| TPC552 | A / 1 | TP-P5 | PP16V0_MESA_CONN | 48 |
| TPC537 | A / 1 | TP-P5 | | |
| TPC554 | A / 1 | TP-P5 | PP3V0_MESA_CONN | 48 120 |
| TPC555 | A / 1 | TP-P5 | PP3V0_MESA_CONN | 48 120 |
| TPC545 | A / 1 | TP-P5 | | |
| TPC553 | A / 1 | TP-P5 | | |

## FAN , Keyboard,Trackpad Test Points

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC556 | A / 1 | TP-P5 | GND_FAN | 65 120 |
| TPC557 | A / 1 | TP-P5 | GND_FAN | 65 120 |
| TPC558 | A / 1 | TP-P5 | PP5V_G3S_FAN_CONN | 65 120 |
| TPC559 | A / 1 | TP-P5 | PP5V_G3S_FAN_CONN | 65 120 |
| TPC560 | A / 1 | TP-P5 | FAN_LT_TACH | 59 65 |
| TPC561 | A / 1 | TP-P5 | FAN_RT_TACH | 59 65 |
| TPC562 | A / 1 | TP-P5 | FAN_LT_PWM | 59 65 |
| TPC563 | A / 1 | TP-P5 | FAN_RT_PWM | 59 65 |
| TPC564 | A / 1 | TP-P5 | | |
| TPC565 | A / 1 | TP-P5 | | |
| TPC5Z1 | A / 1 | TP-P5 | GND_FAN | 65 120 |
| TPC5Z2 | A / 1 | TP-P5 | GND_FAN | 65 120 |
| TPC5Z9 | A / 1 | TP-P5 | I2C_TPAD3V3_SCL | 65 66 |
| TPC5Y0 | A / 1 | TP-P5 | TPAD_KBD_WAKE_L | 47 65 66 |
| TPC566 | A / 1 | TP-P5 | I2C_TPAD3V3_SDA | 65 66 |
| TPC567 | A / 1 | TP-P5 | TPAD3V3_ACTUATOR_DISABLE_L | 65 66 |
| TPC568 | A / 1 | TP-P5 | I2C_KBD_SDA | 65 |
| TPC569 | A / 1 | TP-P5 | TPAD3V3_SPI_INT_L | 65 66 |
| TPC5Z8 | A / 1 | TP-P5 | IPD_LID_OPEN | 47 50 65 |
| TPC5Z3 | A / 1 | TP-P5 | PP5V_G3S | 116 119 120 |
| TPC5Z4 | A / 1 | TP-P5 | PP5V_G3S | 116 119 120 |
| TPC5Z7 | A / 1 | TP-P5 | PMU_RSLOC_RST_R_L | 65 |
| TPC5Z5 | A / 1 | TP-P5 | PP3V3_G3H_RTC_X | 116 |
| TPC571 | A / 1 | TP-P5 | | |
| TPC588 | A / 1 | TP-P5 | ACT_GND | 65 120 |
| TPC586 | A / 1 | TP-P5 | ACT_GND | 65 120 |
| TPC579 | A / 1 | TP-P5 | KBD_BLC_GSSOUT | 65 |
| TPC578 | A / 1 | TP-P5 | TPAD3V3_SPI_EN | 65 66 |
| TPC585 | A / 1 | TP-P5 | PP3V3_G3S_T | 65 116 120 |
| TPC584 | A / 1 | TP-P5 | PP3V3_G3S_T | 65 116 120 |
| TPC583 | A / 1 | TP-P5 | KBD_BLC_GSLAT | 65 |
| TPC582 | A / 1 | TP-P5 | PP5V_G3S_TPAD_CONN | 65 |
| TPC581 | A / 1 | TP-P5 | KBD_BLC_GSSCK | 65 |
| TPC580 | A / 1 | TP-P5 | SPI_TPAD3V3_CLK | 65 66 |
| TPC591 | A / 1 | TP-P5 | PPVIN_G3H_TPAD_FUSE | 65 120 |
| TPC590 | A / 1 | TP-P5 | PPVIN_G3H_TPAD_FUSE | 65 120 |
| TPC589 | A / 1 | TP-P5 | PPVIN_G3H_TPAD_FUSE | 65 120 |
| TPC577 | A / 1 | TP-P5 | KBD_BLC_GSSIN | 65 |
| TPC576 | A / 1 | TP-P5 | SPI_TPAD3V3_MISO | 65 66 |
| TPC575 | A / 1 | TP-P5 | KBD_BLC_XBLANK | 65 |
| TPC574 | A / 1 | TP-P5 | SPI_TPAD3V3_CS_L | 65 66 |
| TPC572 | A / 1 | TP-P5 | SPI_TPAD3V3_MOSI | 65 66 |
| TPC573 | A / 1 | TP-P5 | I2C_KBD_SCL | 65 |
| TPC587 | A / 1 | TP-P5 | | |
| TPC5M0 | A / 1 | TP-P5 | KBD_INT_L | 65 |

## AUDIO

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC592 | A / 1 | TP-P5 | AUD_DMIC0_CLK_CONN | 64 |
| TPC593 | A / 1 | TP-P5 | AUD_DMIC0_DATA_CONN | 64 |
| TPC594 | A / 1 | TP-P5 | PP1V8_DMIC | 64 |
| TPC595 | A / 1 | TP-P5 | AUD_DMIC1_CLK_CONN | 64 |
| TPC596 | A / 1 | TP-P5 | AUD_DMIC1_DATA_CONN | 64 |
| TPC597 | A / 1 | TP-P5 | | |
| TPC5A1 | A / 1 | TP-P5 | SPKRCONN_LW_OUTN | 62 120 |
| TPC5B1 | A / 1 | TP-P5 | SPKRCONN_LW_OUTN | 62 120 |
| TPC5B4 | A / 1 | TP-P5 | SPKRCONN_LW_OUTN | 62 120 |
| TPC5A0 | A / 1 | TP-P5 | SPKRCONN_LW_OUTP | 62 120 |
| TPC5G0 | A / 1 | TP-P5 | SPKRCONN_LW_OUTP | 62 120 |
| TPC5G1 | A / 1 | TP-P5 | SPKRCONN_LW_OUTP | 62 120 |
| TPC598 | A / 1 | TP-P5 | SPKRCONN_LT_OUTN | 62 120 |
| TPC5G2 | A / 1 | TP-P5 | SPKRCONN_LT_OUTN | 62 120 |
| TPC5M3 | A / 1 | TP-P5 | SPKRCONN_LT_OUTN | 62 120 |
| TPC599 | A / 1 | TP-P5 | SPKRCONN_LT_OUTP | 62 120 |
| TPC5M4 | A / 1 | TP-P5 | SPKRCONN_LT_OUTP | 62 120 |
| TPC5M5 | A / 1 | TP-P5 | SPKRCONN_LT_OUTP | 62 120 |
| TPC5A6 | A / 1 | TP-P5 | SPKRCONN_RW_OUTP | 63 120 |
| TPC5G6 | A / 1 | TP-P5 | SPKRCONN_RW_OUTP | 63 120 |
| TPC5M7 | A / 1 | TP-P5 | SPKRCONN_RW_OUTP | 63 120 |
| TPC5Y9 | A / 1 | TP-P5 | SPKRCONN_RW_OUTN | 63 120 |
| TPC5G8 | A / 1 | TP-P5 | SPKRCONN_RW_OUTN | 63 120 |
| TPC5M9 | A / 1 | TP-P5 | SPKRCONN_RW_OUTN | 63 120 |
| TPC5A3 | A / 1 | TP-P5 | SPKRCONN_RT_OUTN | 63 120 |
| TPC5L3 | A / 1 | TP-P5 | SPKRCONN_RT_OUTN | 63 120 |
| TPC5L4 | A / 1 | TP-P5 | SPKRCONN_RT_OUTN | 63 120 |
| TPC5A4 | A / 1 | TP-P5 | SPKRCONN_RT_OUTP | 63 120 |
| TPC5L5 | A / 1 | TP-P5 | SPKRCONN_RT_OUTP | 63 120 |
| TPC5L6 | A / 1 | TP-P5 | SPKRCONN_RT_OUTP | 63 120 |
| TPC5B8 | A / 1 | TP-P5 | AUD_CONN_RING_SENSE | 64 |
| TPC5B7 | A / 1 | TP-P5 | AUD_CONN_RING2_XW | 64 119 |
| TPC5B6 | A / 1 | TP-P5 | AUD_CONN_TIP_SENSE | 64 119 |
| TPC5B5 | A / 1 | TP-P5 | AUD_CONN_HP_SENSE_R | 64 119 |
| TPC5A7 | A / 1 | TP-P5 | | |
| TPC5B3 | A / 1 | TP-P5 | AUD_CONN_HP_SENSE_L | 64 119 |
| TPC5A8 | A / 1 | TP-P5 | AUD_CONN_HP_LEFT | 64 119 |
| TPC5A9 | A / 1 | TP-P5 | AUD_CONN_HP_RIGHT | 64 119 |
| TPC5B0 | A / 1 | TP-P5 | AUD_CONN_RING2 | 64 119 |
| TPC5B2 | A / 1 | TP-P5 | AUD_CONN_SLEEVE | 64 119 |
| TPC5K0 | A / 1 | TP-P5 | | |
| TPC5K1 | A / 1 | TP-P5 | AUD_CONN_SLEEVE_XW | 64 119 |
| TPC5A5 | A / 1 | TP-P5 | SPKR_ID0 | 40 63 |
| TPC5A2 | A / 1 | TP-P5 | | |

## USBC (PLACE NEAR CONNECTOR)

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5G3 | A / 1 | TP-P5 | TP_USBC_PP20V_XB | 32 |
| TPC5N3 | A / 1 | TP-P5 | TP_USBC_PP20V_XA | 32 |
| TPC5G4 | A / 1 | TP-P5 | USBC_XA_SBU1 | 30 32 |
| TPC5G5 | A / 1 | TP-P5 | USBC_XA_SBU2 | 30 32 |
| TPC5G7 | A / 1 | TP-P5 | USBC_XA_CC2_CONN | 32 33 |
| TPC5G9 | A / 1 | TP-P5 | PP20V_USBC_XB_VBUS | 29 32 120 122 |
| TPC5H0 | A / 1 | TP-P5 | PP20V_USBC_XA_VBUS | 29 32 119 120 122 |
| TPC5H1 | A / 1 | TP-P5 | TP_USBC_PP20V_TB | 110 |
| TPC5H2 | A / 1 | TP-P5 | TP_USBC_PP20V_TA | 110 |
| TPC5H3 | A / 1 | TP-P5 | PP20V_USBC_TB_VBUS | 107 110 120 122 |
| TPC5H4 | A / 1 | TP-P5 | PP20V_USBC_TA_VBUS | 107 110 120 122 |
| TPC5I8 | A / 1 | TP-P5 | PP20V_USBC_XA_VBUS | 29 32 119 120 122 |
| TPC5I9 | A / 1 | TP-P5 | PP20V_USBC_XA_VBUS | 29 32 119 120 122 |
| TPC5J1 | A / 1 | TP-P5 | PP20V_USBC_XB_VBUS | 29 32 120 122 |
| TPC5J0 | A / 1 | TP-P5 | PP20V_USBC_XA_VBUS | 29 32 119 120 122 |
| TPC5J2 | A / 1 | TP-P5 | PP20V_USBC_XB_VBUS | 29 32 120 122 |
| TPC5J3 | A / 1 | TP-P5 | PP20V_USBC_XB_VBUS | 29 32 120 122 |
| TPC5J4 | A / 1 | TP-P5 | PP20V_USBC_TA_VBUS | 107 110 120 122 |
| TPC5H5 | A / 1 | TP-P5 | | |
| TPC5H6 | A / 1 | TP-P5 | | |
| TPC5H7 | A / 1 | TP-P5 | | |
| TPC5H8 | A / 1 | TP-P5 | | |
| TPC5M2 | A / 1 | TP-P5 | | |
| TPC5K2 | A / 1 | TP-P5 | | |
| TPC5K3 | A / 1 | TP-P5 | | |
| TPC5K4 | A / 1 | TP-P5 | | |
| TPC5J5 | A / 1 | TP-P5 | PP20V_USBC_TA_VBUS | 107 110 120 122 |
| TPC5J6 | A / 1 | TP-P5 | PP20V_USBC_TA_VBUS | 107 110 120 122 |
| TPC5J7 | A / 1 | TP-P5 | PP20V_USBC_TB_VBUS | 107 110 120 122 |
| TPC5J8 | A / 1 | TP-P5 | PP20V_USBC_TB_VBUS | 107 110 120 122 |
| TPC5J9 | A / 1 | TP-P5 | PP20V_USBC_TB_VBUS | 107 110 120 122 |
| TPC5N9 | A / 1 | TP-P5 | USBC_XB_CC1_CONN | 32 33 |
| TPC5N8 | A / 1 | TP-P5 | USBC_XB_CC2_CONN | 32 33 |
| TPC5O1 | A / 1 | TP-P5 | USBC_TA_CC1_CONN | 110 111 |
| TPC5O2 | A / 1 | TP-P5 | USBC_TA_CC2_CONN | 110 111 |
| TPC5O3 | A / 1 | TP-P5 | USBC_TB_CC1_CONN | 110 111 |
| TPC5O4 | A / 1 | TP-P5 | USBC_TB_CC2_CONN | 110 111 |

CORE OS DESBUG

## TBT/DP

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5L7 | A / 1 | TP-P5 | TBT_X_HDMI_DDC_DATA | 29 95 |
| TPC5L8 | A / 1 | TP-P5 | TBT_X_HDMI_DDC_CLK | 29 95 |
| TPC5L9 | A / 1 | TP-P5 | TBT_T_HDMI_DDC_DATA | 95 107 |
| TPC5N0 | A / 1 | TP-P5 | TBT_T_HDMI_DDC_CLK | 95 107 |

## WIRELESS

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5H9 | A / 1 | TP-P5 | PP3V3_G3S_WLAN | 116 |
| TPC5I0 | A / 1 | TP-P5 | PP1V8_G3S_WLANBT_VDDIO | 116 |
| TPC5L0 | A / 1 | TP-P5 | PPVIN_RFLDO_WLANBT | 36 122 |
| TPC5L1 | A / 1 | TP-P5 | PP1V2_WLANBT | 36 122 |
| TPC5L2 | A / 1 | TP-P5 | PP1V5_WLANBT | 36 122 |

## HALL EFFECT

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5I1 | A / 1 | TP-P5 | LID_OPEN_LEFT | 47 64 |
| TPC5I2 | A / 1 | TP-P5 | LID_OPEN_RIGHT | 47 64 |

## MEMORY

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5I3 | A / 1 | TP-P5 | PVDDQ_PGOOD | 74 77 |
| TPC5I7 | A / 1 | TP-P5 | PP1V2_S3_CPUDDR | 115 |

## EDP , CAMERA,ALS

| Test Point | Pin | Part | Net | Pages |
|---|---|---|---|---|
| TPC5C0 | A / 1 | TP-P5 | EDP_INT_AUX_N | 82 93 |
| TPC5C1 | A / 1 | TP-P5 | | |
| TPC5C2 | A / 1 | TP-P5 | EDP_INT_AUX_P | 82 93 |
| TPC5C3 | A / 1 | TP-P5 | EDP_PANEL_PWR_BUF_EN | 82 |
| TPC5C4 | A / 1 | TP-P5 | | |
| TPC5C9 | A / 1 | TP-P5 | TP_LCD_IRQ_L | 82 |
| TPC5C8 | A / 1 | TP-P5 | EDP_INT_ML_P<0> | 82 93 |
| TPC5C5 | A / 1 | TP-P5 | DP_INT_HPD | 82 93 |
| TPC5C6 | A / 1 | TP-P5 | EDP_INT_ML_N<0> | 82 93 |
| TPC5C7 | A / 1 | TP-P5 | LCD_FSS | 82 93 |
| TPC5D5 | A / 1 | TP-P5 | EDP_INT_ML_P<2> | 82 93 |
| TPC5D3 | A / 1 | TP-P5 | EDP_INT_ML_N<2> | 82 93 |
| TPC5D1 | A / 1 | TP-P5 | EDP_INT_ML_N<1> | 82 93 |
| TPC5D2 | A / 1 | TP-P5 | EDP_INT_ML_P<1> | 82 93 |
| TPC5D0 | A / 1 | TP-P5 | | |
| TPC5D7 | A / 1 | TP-P5 | I2C_BKLT_SDA | 81 82 |
| TPC5E0 | A / 1 | TP-P5 | EDP_INT_ML_P<3> | 82 93 |
| TPC5D9 | A / 1 | TP-P5 | I2C_BKLT_SCL | 81 82 |
| TPC5D8 | A / 1 | TP-P5 | EDP_INT_ML_N<3> | 82 93 |
| TPC5D4 | A / 1 | TP-P5 | | |
| TPC5E1 | A / 1 | TP-P5 | I2C_TCON_SDA | 51 82 |
| TPC5E4 | A / 1 | TP-P5 | MIPI_FTCAM_DATA_CONN_N<0> | 82 |
| TPC5D6 | A / 1 | TP-P5 | | |
| TPC5E3 | A / 1 | TP-P5 | I2C_TCON_SCL | 51 82 |
| TPC5F2 | A / 1 | TP-P5 | I2C_CAM_ISOL_SDA | 82 |
| TPC5F1 | A / 1 | TP-P5 | MIPI_FTCAM_CLK_CONN_P | 82 |
| TPC5F0 | A / 1 | TP-P5 | I2C_CAM_ISOL_SCL | 82 |
| TPC5E9 | A / 1 | TP-P5 | MIPI_FTCAM_CLK_CONN_N | 82 |
| TPC5E8 | A / 1 | TP-P5 | I2C_ALS_SCL | 40 52 |
| TPC5E2 | A / 1 | TP-P5 | | |
| TPC5E6 | A / 1 | TP-P5 | MIPI_FTCAM_DATA_CONN_P<0> | 82 |
| TPC5E7 | A / 1 | TP-P5 | I2C_ALS_SDA | 40 52 |
| TPC5F7 | A / 1 | TP-P5 | PP5V_S0_ALSCAM_F | 82 |
| TPC5E5 | A / 1 | TP-P5 | | |
| TPC5F9 | A / 1 | TP-P6 | PPVIN_S0SW_LCDBKLT_R | 81 |
| TPC5F3 | A / 1 | TP-P5 | PPVOUT_S0_LCDBKLT | 81 82 122 |
| TPC5F4 | A / 1 | TP-P5 | PP3V3_S0SW_LCD | 51 82 120 |
| TPC5F6 | A / 1 | TP-P5 | PP5V_S0SW_LCD | 82 |
| TPC5F5 | A / 1 | TP-P5 | PP3V3_S0SW_LCD | 51 82 120 |
| TPC5F8 | A / 1 | TP-P5 | | |
| TPC5M1 | A / 1 | TP-P5 | BKLT_PWM_MLB2TCON | 82 |

PAGE TITLE: FCT TESTPOINTS 2

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# ICT TEST POINTS, ICT BOUNDARY SCAN TESTPOINTS

## CPU XDP and PCH Test-Points

| | | | |
|---|---|---|---|
| 18 6 | IN | TRUE | XDP_CPU_TCK |
| 18 13 | IN | TRUE | XDP_PCH_TCK |
| 18 6 | IN | TRUE | XDP_CPU_TDI |
| 18 6 | IN | TRUE | XDP_CPU_TDO |
| 18 13 6 | IN | TRUE | XDP_CPU_TRST_L |
| 18 6 | IN | TRUE | XDP_CPU_TMS |
| 18 13 | IN | TRUE | XDP_PCH_TMS |
| 18 13 | IN | TRUE | XDP_PCH_TDI |
| 18 13 | IN | TRUE | XDP_PCH_TDO |
| 18 13 6 | IN | TRUE | XDP_CPU_PREQ_L |
| 18 13 6 | IN | TRUE | XDP_CPU_PRDY_L |
| 119 46 35 12 | IN | TRUE | PM_PCH_PWROK |
| 119 46 18 12 | IN | TRUE | PM_SYSRST_L |
| 18 13 | IN | TRUE | XDP_PCH_JTAGX |
| 18 13 | BI | | PCH_ITP_PMODE FUNC_TEST=TRUE |

H9M BOUNDARY SCAN TESTPOINTS ON FCT TESTPOINT PAGE

## TP Debug ACE Nets (EE tests)

| | | |
|---|---|---|
| 30 | UPC_XA_GPIO0 | TPC622 |
| 31 | UPC_XB_GPIO0 | TPC624 |
| 31 | UPC_XB_GPIO1 | TPC625 |
| 108 | UPC_TA_GPIO0 | TPC626 |
| 108 | UPC_TA_GPIO1 | TPC627 |
| 109 | UPC_TB_GPIO0 | TPC628 |
| 109 | UPC_TB_GPIO1 | TPC629 |

## GPU ICT TESTPONTS

ACE

| | | | |
|---|---|---|---|
| 27 15 | BI | JTAG_TBT_X_TMS | FUNC_TEST=TRUE |
| 107 105 27 | BI | JTAG_ISP_TDI | FUNC_TEST=TRUE |
| 107 105 27 | BI | JTAG_ISP_TCK | FUNC_TEST=TRUE |
| 107 105 27 | BI | XDP_JTAG_ISP_TDO | FUNC_TEST=TRUE |
| 121 27 | BI | TBT_X_TEST_EN | FUNC_TEST=TRUE |

WLAN

| | | | |
|---|---|---|---|
| 39 37 | BI | WLAN_JTAG_TMS | FUNC_TEST=TRUE |
| 39 37 | BI | WLAN_JTAG_TCK | FUNC_TEST=TRUE |
| 40 37 | BI | WLAN_JTAG_TDI | FUNC_TEST=TRUE |
| 37 36 | BI | WLAN_JTAG_TDO | FUNC_TEST=TRUE |
| 37 36 | BI | WLAN_JTAG_TRST_L | FUNC_TEST=TRUE |
| 105 15 | BI | JTAG_TBT_T_TMS | FUNC_TEST=TRUE |
| 39 | BI | TP_JTAG_SOC_TRST_L | FUNC_TEST=TRUE |

GPU

| | | | |
|---|---|---|---|
| 103 102 | BI | GPU_JTAG_TCK | FUNC_TEST=TRUE |
| 103 102 | BI | GPU_JTAG_TDI | FUNC_TEST=TRUE |
| 103 102 | BI | GPU_JTAG_TDO | FUNC_TEST=TRUE |
| 103 102 | BI | GPU_JTAG_TMS | FUNC_TEST=TRUE |
| 103 102 | BI | GPU_JTAG_TRST_L | FUNC_TEST=TRUE |
| 46 39 | BI | SMC_PCH_SYS_PWROK | FUNC_TEST=TRUE |
| 46 39 | BI | SMC_PCH_PWROK | FUNC_TEST=TRUE |
| 119 46 39 | BI | SMC_SYSRST_L | FUNC_TEST=TRUE |
| 119 13 6 | BI | CPU_PWRGD | FUNC_TEST=TRUE |
| 77 64 39 119 | BI | PMU_COLD_RESET_L | FUNC_TEST=TRUE |
| 39 | BI | SOC_JTAG_SEL | FUNC_TEST=TRUE |
| 38 | BI | SOC_TESTMODE | FUNC_TEST=TRUE |
| 37 36 | BI | WLAN_JTAG_SEL | FUNC_TEST=TRUE |
| 105 | BI | TBT_T_TEST_EN | FUNC_TEST=TRUE |
| 121 27 | BI | TBT_X_TEST_EN | FUNC_TEST=TRUE |

## SSD BOUNDARY SCAN Test-Points

| | | | |
|---|---|---|---|
| 85 84 83 39 86 | IN | TRUE | SSD0_SWDIO_UART_D2R |
| 85 84 83 39 86 | IN | TRUE | SSD0_SWCLK_UART_R2D |
| 84 83 | IN | TRUE | SSD0_S4E0_JTAG_TDO |
| 83 | IN | TRUE | SSD0_S4E0_JTAG_TDI |
| 86 85 84 83 | IN | TRUE | SSD0_S4E_JTAG_SEL |
| 85 84 | IN | TRUE | SSD0_S4E1_JTAG_TDO |
| 121 86 85 | IN | TRUE | SSD0_S4E2_JTAG_TDO |
| 86 | IN | | SSD0_S4E3_JTAG_TDO |
| 121 86 85 | IN | TRUE | SSD0_S4E2_JTAG_TDO |
| 90 89 88 39 91 | IN | TRUE | SSD1_SWDIO_UART_D2R |
| 90 89 88 39 91 | IN | TRUE | SSD1_SWCLK_UART_R2D |
| 89 88 | IN | TRUE | SSD1_S4E0_JTAG_TDO |
| 88 | IN | TRUE | SSD1_S4E0_JTAG_TDI |
| 91 90 89 88 | IN | TRUE | SSD1_S4E_JTAG_SEL |
| 90 89 | IN | TRUE | SSD1_S4E1_JTAG_TDO |
| 91 90 | IN | TRUE | SSD1_S4E2_JTAG_TDO |
| 91 89 | IN | TRUE | SSD1_S4E3_JTAG_TDO |

## S4E

| | | | |
|---|---|---|---|
| PPC603 | PP | 1 P3MM SM | PVDDCPUAWAKE_SW0 75 |
| PPC604 | PP | 1 P3MM SM | PVDDCPUAWAKE_SW1 75 |
| PPC605 | PP | 1 P3MM SM | PVDDCPUAWAKE_SW2 75 |
| PPC606 | PP | 1 P3MM SM | PVDDCPUAWAKE_SW3 75 |
| PPC607 | PP | 1 P3MM SM | PVCCPRIMCORE_SW0 75 |
| PPC608 | PP | 1 P3MM SM | PVCCPRIMCORE_SW1 75 |
| PPC609 | PP | 1 P3MM SM | P0V8SLPDDR_SW0 75 |
| PPC610 | PP | 1 P3MM SM | P0V8SLPDDR_SW1 75 |
| PPC611 | PP | 1 P3MM SM | P1V8SLPS2R_SW0 75 |
| PPC612 | PP | 1 P3MM SM | P1V1SLPS2R_SW0 75 |
| PPC613 | PP | 1 P3MM SM | P1V1SLPS2R_SW1 75 |
| PPC614 | PP | 1 P3MM SM | P0V9SLPDDR_SW0 75 |
| PPC615 | PP | 1 P3MM SM | P0V9SLPDDR_SW1 75 |
| PPC616 | PP | 1 P3MM SM | PVDDCPUSRAMAWAKE_SW0 75 |

## EE TESTS SWE

| | | |
|---|---|---|
| 53 | ISNS_HS_COMPUTING_P | TPC650 |
| 53 | ISNS_HS_COMPUTING_N | TPC651 |
| 53 | ISNS_HS_OTHER5V_P | TPC652 |
| 53 | ISNS_HS_OTHER5V_N | TPC653 |
| 53 | ISNS_HS_3V3_X_P | TPC654 |
| 53 | ISNS_HS_3V3_X_N | TPC655 |
| 53 | ISNS_HS_3V3_T_P | TPC656 |
| 53 | ISNS_HS_3V3_T_N | TPC657 |
| 81 53 | ISNS_LCDBKLT_P | TPC658 |
| 81 53 | ISNS_LCDBKLT_N | TPC659 |
| 54 | ISNS_1V0_P | TPC660 |
| 54 | ISNS_1V0_N | TPC661 |
| 74 54 | ISNS_CPUDDR_P | TPC662 |
| 74 54 | ISNS_CPUDDR_N | TPC663 |
| 54 | ISNS_CPUVDDQ_P | TPC664 |
| 54 | ISNS_CPUVDDQ_N | TPC665 |
| 54 | CPUVR_ISNS_P | TPC666 |
| 54 | CPUVR_ISNS_N | TPC667 |
| 54 | ISNS_WLAN_N | TPC668 |
| 54 | ISNS_WLAN_P | TPC669 |
| 54 | ISNS_WL1V8_P | TPC670 |
| 54 | ISNS_WL1V8_N | TPC671 |
| 82 55 | ISNS_LCDPANEL_P | TPC672 |
| 82 55 | ISNS_LCDPANEL_N | TPC673 |
| 56 | ISNS_CALPE_P | TPC674 |
| 56 | ISNS_CALPE_N | TPC675 |
| 56 | CPUGT_ISNS_R_P | TPC676 |
| 56 | CPUGT_ISNS_R_N | TPC677 |
| 71 56 | CPUSA_ISNS_P | TPC678 |
| 71 56 | CPUSA_ISNS_N | TPC679 |
| 78 56 | ISNS_CPUVCCIO_POS | TPC680 |
| 78 56 | ISNS_CPUVCCIO_NEG | TPC681 |
| 94 | GFXIMVP_ISNS_R_N | TPC682 |
| 94 | GFXIMVP_ISNS_R_P | TPC683 |
| 98 58 | VDDCIS0_CS_P | TPC684 |
| 98 58 | VDDCIS0_CS_N | TPC685 |
| 58 | ISNS_GPU1V8_P | TPC686 |
| 58 | ISNS_GPU1V8_N | TPC687 |
| 98 58 | GPUFB_CS_P | TPC688 |
| 98 58 | GPUFB_CS_N | TPC689 |
| 58 | ISNS_GPUFBIC_P | TPC6A0 |
| 58 | ISNS_GPUFBIC_N | TPC6A1 |
| 58 | ISNS_GPU_HS_P | TPC6A2 |
| 58 | ISNS_GPU_HS_N | TPC6A3 |
| 59 53 | SMC_PBUS_VSENSE | TPC6A4 |
| 59 58 | PMU_CPU_VSENSE | TPC6A5 |
| 59 58 | PMU_GPU_CORE_VSENSE | TPC6A6 |
| 58 56 | EADC1_CPUGT_VSENSE | TPC6A7 |
| 72 62 64 52 58 84 | GND_CALPE_AVSS | TPC6A8 |
| 58 56 | EADC1_CPUSA_VSENSE | TPC6A9 |
| 58 56 | EADC2_GPU_VDDCI_VSENSE | TPC6B0 |
| 55 54 58 56 | GND_EADC2_COM | TPC6B1 |
| 59 53 | SMC_DCIN_VSENSE | TPC6B2 |
| 68 | CHGR_CSI_R_P | TPC6B3 |
| 68 | CHGR_CSI_R_N | TPC6B4 |
| 68 55 | CHGR_CSO_R_P | TPC6B5 |
| 68 55 | CHGR_CSO_R_N | TPC6B6 |
| 55 | ISNS_PPBUS_MAIN_SSD0_P | TPC6B7 |
| 55 | ISNS_PPBUS_MAIN_SSD0_N | TPC6B8 |
| 55 | ISNS_PPBUS_MAIN_SSD1_P | TPC6B9 |

## EE TESTS SWE -2

| | | |
|---|---|---|
| 55 | ISNS_PPBUS_MAIN_SSD1_N | TPC6C0 |
| 55 | ISNS_P3V3_G3W_SSD0_P | TPC6C1 |
| 55 | ISNS_P3V3_G3W_SSD0_N | TPC6C2 |
| 55 | ISNS_P3V3_G3W_SSD1_P | TPC6C3 |
| 55 | ISNS_P3V3_G3W_SSD1_N | TPC6C4 |
| 55 | ISNS_T139_P | TPC6C7 |
| 55 | ISNS_T139_N | TPC6C8 |

## WP pins of ROMs

| | | | |
|---|---|---|---|
| 36 | BT_SFLASH_WP_L | TPC6D0 | PLACE_SIDE=TOP |
| 27 | TBT_X_ROM_WP_L | TPC6D1 | PLACE_SIDE=TOP |
| 105 | TBT_T_ROM_WP_L | TPC6D2 | PLACE_SIDE=TOP |
| 102 | GPU_ROM_WP_L | TPC6D3 | PLACE_SIDE=TOP |
| 46 | SPI_SOCROM_WP_L | TPC6D4 | PLACE_SIDE=TOP |

## EE TESTS PCH

| | | | |
|---|---|---|---|
| 12 | PCIE_CLK100M_DEBUG_N | TPC620 | PLACE_NEAR=U1200.AK6:25MM |
| 12 | PCIE_CLK100M_DEBUG_P | TPC621 | PLACE_NEAR=U1200.AM6:25MM |
| 36 12 | PCH_PCIE_CLK100M_WLAN_N | TPC631 | |
| 36 12 | PCH_PCIE_CLK100M_WLAN_P | TPC632 | |
| 41 12 | PCIE_CLK100M_SOC_N | PPC633 | PLACE_NEAR=U3900.G12:25MM |
| 41 12 | PCIE_CLK100M_SOC_P | PPC634 | PLACE_NEAR=U3900.G13:25MM |

## S4E

| | | | |
|---|---|---|---|
| TPC690A | SSD0_S4E0_UART_TX | SSD1_S4E0_UART_TX | 83 |
| TPC691A | SSD1_S4E0_UART_TX | SSD0_S4E1_UART_TX | 88 |
| TPC692A | SSD0_S4E1_UART_TX | SSD1_S4E1_UART_TX | 84 |
| TPC693A | SSD1_S4E1_UART_TX | SSD0_S4E2_UART_TX | 89 |
| TPC694A | SSD0_S4E2_UART_TX | SSD0_S4E3_UART_TX | 85 |
| TPC695A | SSD0_S4E3_UART_TX | SSD1_S4E3_UART_TX | 86 |
| TPC696A | SSD1_S4E3_UART_TX | SSD0_S4E1_DROOP_L | 91 |
| TPC697A | SSD1_S4E2_UART_TX | SSD0_S4E2_UART_TX | 84 |
| TPC698A | SSD0_CLKREQ2_L | | 90 |
| TPC699A | SSD0_S4E3_DROOP_L | | 41 47 85 |
| TPC69AA | SSD0_S4E2_DROOP_L | | 86 |
| TPC69BA | SSD0_CLKREQ3_L | | 85 |
| TPC69CA | SSD0_S4E0_DROOP_L | | 41 47 86 |
| TPC69DA | | | 83 |

PAGE TITLE: ICT, MAC-1 ,EE Testpoints

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BRANCH: 126 OF 200

PAGE

SHEET: 121 OF 131

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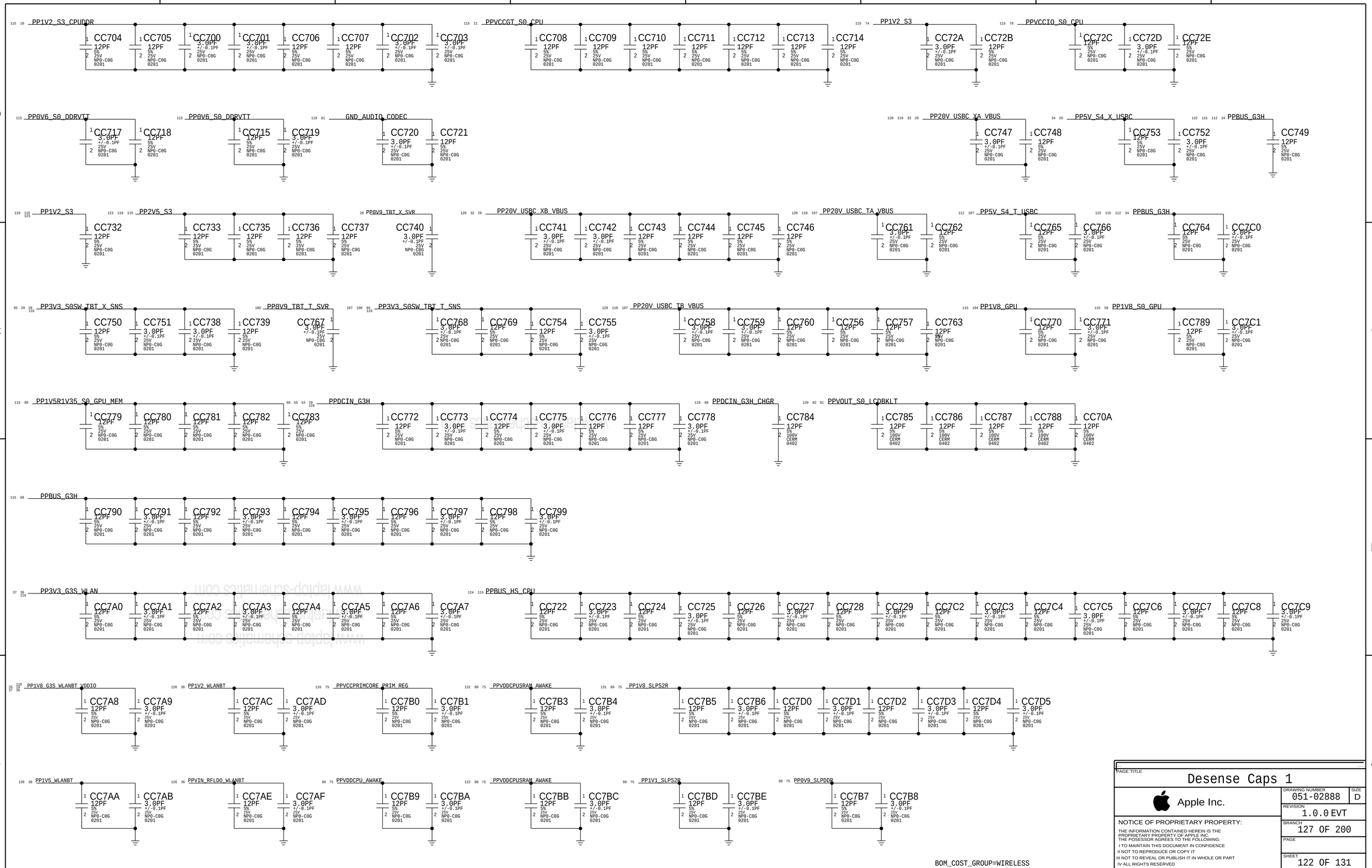


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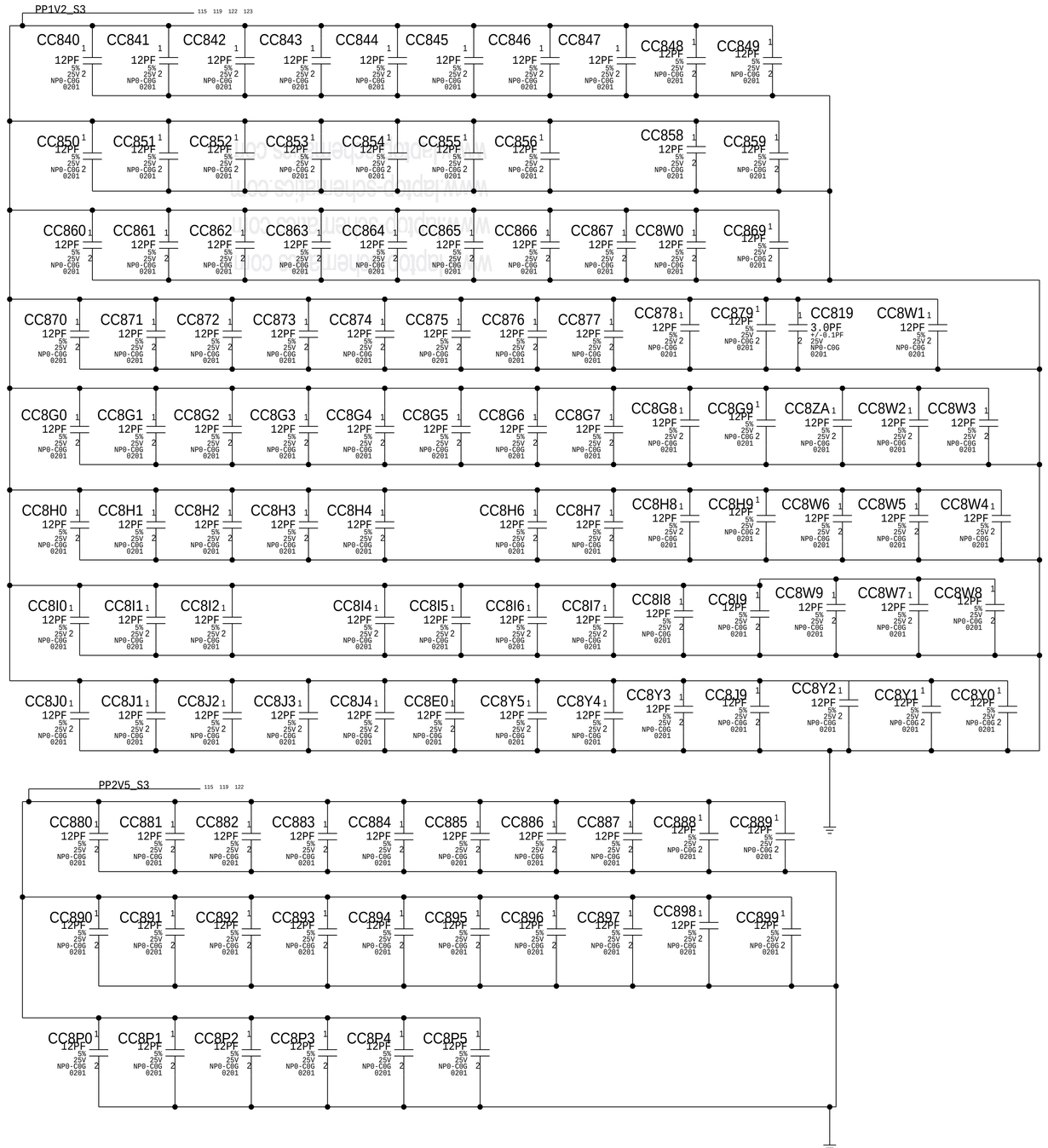


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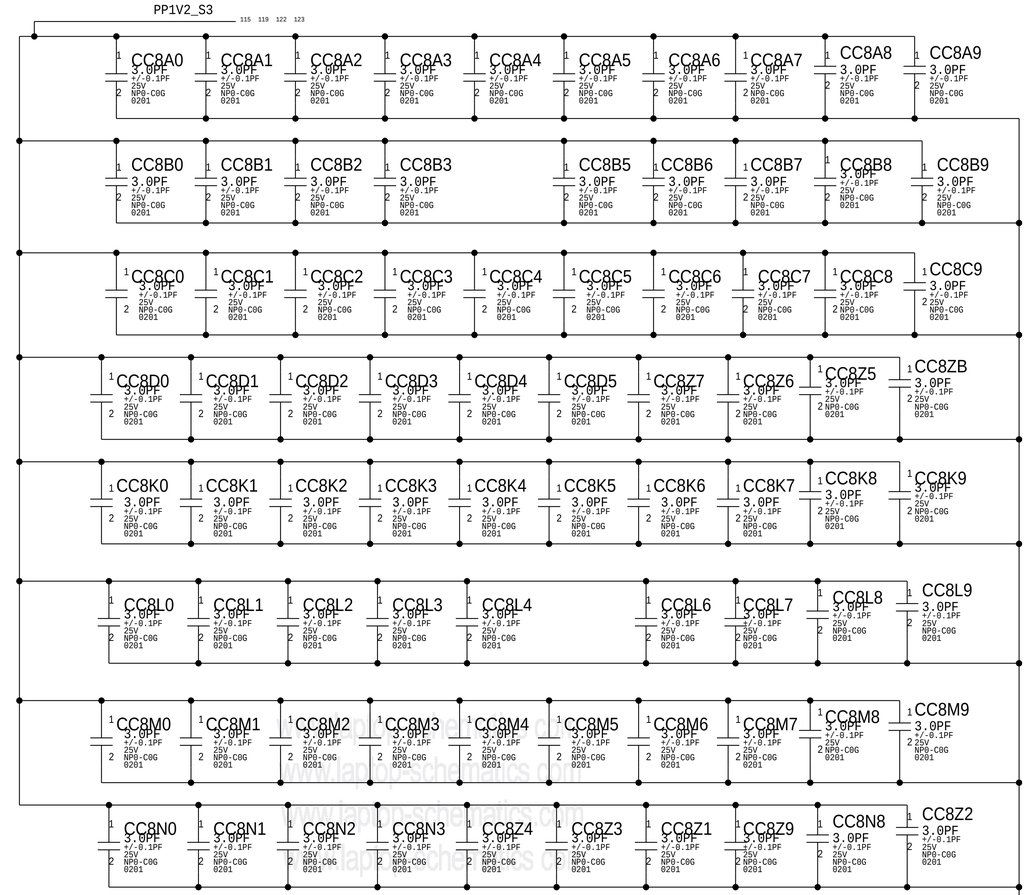


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| PAGE TITLE | Desense Caps 2 |
| Apple Inc. | DRAWING NUMBER 051-02888 SIZE D |
| | REVISION 1.0.0 EVT |
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| | PAGE |
| | SHEET 123 OF 131 |

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Near NAND IC's

PP1V8_SSD0: CC900 12PF, CC901 3.0PF, CC902 12PF, CC903 3.0PF, CC904 12PF, CC905 3.0PF, CC906 12PF, CC907 3.0PF

Near NAND IC's

PP1V8_SSD1: CC918 12PF, CC919 3.0PF, CC91A 12PF, CC91B 3.0PF, CC91C 12PF, CC91D 3.0PF, CC91E 12PF, CC91F 3.0PF

Near NAND VR's

PP1V8_SSD0: CC930 12PF, CC931 3.0PF

PP1V8_SSD1: CC932 12PF, CC933 3.0PF

PP0V9_SSD0: CC908 12PF, CC909 3.0PF, CC90A 12PF, CC90B 3.0PF, CC90C 12PF, CC90D 3.0PF, CC90E 12PF, CC90F 3.0PF

PP0V9_SSD1: CC920 12PF, CC921 3.0PF, CC922 12PF, CC923 3.0PF, CC924 12PF, CC925 3.0PF, CC926 12PF, CC927 3.0PF

PP0V9_SSD0: CC934 12PF, CC935 3.0PF

PP0V9_SSD1: CC936 12PF, CC937 3.0PF

PP2V5_NAND_SSD0: CC910 12PF, CC911 3.0PF, CC912 12PF, CC913 3.0PF, CC914 12PF, CC915 3.0PF, CC916 12PF, CC917 3.0PF

PP2V5_NAND_SSD1: CC928 12PF, CC929 3.0PF, CC92A 12PF, CC92B 3.0PF, CC92C 12PF, CC92D 3.0PF, CC92E 12PF, CC92F 3.0PF

PP2V5_NAND_SSD0: CC938 12PF, CC939 3.0PF

PP2V5_NAND_SSD1: CC93A 12PF, CC93B 3.0PF

Near GMUX

PP3V3_S5: CC93C 12PF, CC93D 3.0PF, CC93E 12PF, CC93F 3.0PF

Near VRAMS

PP1V5R1V35_S0_GPU_MEM: CC940 12PF, CC941 3.0PF, CC942 12PF, CC943 3.0PF, CC944 12PF, CC945 3.0PF, CC946 12PF, CC947 3.0PF, CC948 12PF, CC949 3.0PF, CC94A 12PF, CC94B 3.0PF, CC94C 12PF, CC94D 3.0PF, CC94E 12PF, CC94F 3.0PF

Near GPU

PP1V5R1V35_S0_GPU_IC: CC950 12PF, CC951 3.0PF, CC952 12PF, CC953 3.0PF

Near GPU

PPVCORE_S0_GPU: CC954 12PF, CC955 3.0PF, CC956 12PF, CC957 3.0PF, CC958 12PF, CC959 3.0PF, CC95A 12PF, CC95B 3.0PF, CC95C 12PF, CC95D 3.0PF, CC95E 12PF, CC95F 3.0PF

Near GPU

PP1V8_S0_GPU_LC_IC: CC960 12PF, CC961 3.0PF, CC962 12PF, CC963 3.0PF

Near GPU

PPVDDCI_S0_GPU: CC964 12PF, CC965 3.0PF, CC966 12PF, CC967 3.0PF, CC968 12PF, CC969 3.0PF, CC96A 12PF, CC96B 3.0PF, CC96C 12PF, CC96D 3.0PF, CC96E 12PF, CC96F 3.0PF

Near Power Shape Top Side

PPBUS_HS_CPU: CC970 12PF, CC971 3.0PF, CC972 12PF, CC973 3.0PF, CC974 12PF, CC975 3.0PF, CC976 12PF, CC977 3.0PF, CC978 12PF, CC979 3.0PF, CC97A 12PF, CC97B 3.0PF

PPBUS_HS_GPU: CC97C 12PF, CC97D 3.0PF, CC97E 12PF, CC97F 3.0PF, CC980 12PF, CC981 3.0PF

GFXIMVP_LGATE1: CC987 3.0PF

GFXIMVP_PHASE2: CC988 3.0PF

GFXIMVP_PHASE3: CC98B 3.0PF

PPVCORE_S0_GPU: CC98C 3.0PF

GFXIMVP_PHASE1: CC989 3.0PF

PPVCORE_S0_GFX_PH1: CC98D 3.0PF

PPVCORE_S0_GFX_PH2: CC98E 3.0PF

PPVCORE_S0_GFX_PH3: CC98F 3.0PF

BOM_COST_GROUP=WIRELESS

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PAGE TITLE: Desense Caps 3

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DRAWING NUMBER: 051-02888 SIZE: D

REVISION: 1.0.0 EVT

BRANCH: 129 OF 200

PAGE

SHEET: 124 OF 131

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# Memory Bit/Byte Swizzle

## DDR4 COMMAND/ADDRESS

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| TRUE | MEM_B_DQS_P<7> | MEM_B_DQS_P<7> |
| TRUE | MEM_B_DQS_N<7> | MEM_B_DQS_N<7> |

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PAGE TITLE
Memory Bite/Byte Swizzle

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DRAWING NUMBER 051-02888 SIZE D
REVISION 1.0.0 EVT
BRANCH 130 OF 200
PAGE
SHEET 125 OF 131

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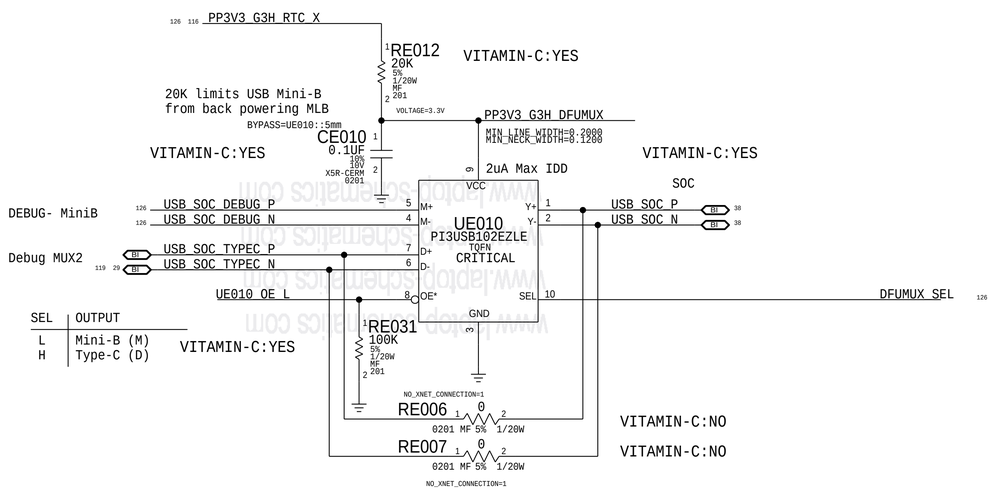
# SoC USB DFU Mux

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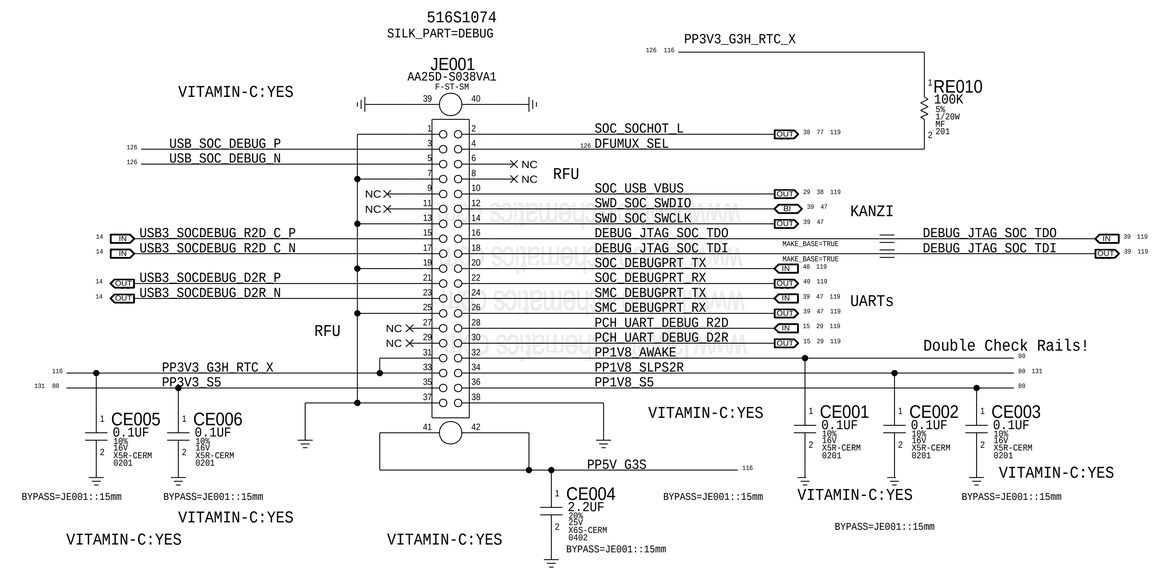


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SYNC_MASTER=Debug SYNC_DATE=05/03/2017

PAGE TITLE

# Dev Support

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DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 140 OF 200

PAGE

SHEET 126 OF 131

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| DRAWING NUMBER 051-02888 | SIZE D |
| REVISION 1.0.0 EVT | |
| BRANCH 141 OF 200 | |
| PAGE | |
| SHEET 127 OF 131 | |

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PAGE TITLE

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DRAWING NUMBER 051-02888

SIZE D

REVISION 1.0.0 EVT

BRANCH 143 OF 200

PAGE

SHEET 128 OF 131

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|---|---|
| DRAWING NUMBER 051-02888 | SIZE D |
| REVISION 1.0.0 EVT | |
| BRANCH 144 OF 200 | |
| PAGE | |
| SHEET 129 OF 131 | |

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# Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 197S00046 | 197S00036 | | ALL | Epson w/ TXC |
| 197S00047 | 197S00036 | | ALL | Kyocera w/ TXC |
| 197S00048 | 197S00036 | | ALL | Murata w/ TXC |
| 376S1080 | 376S0820 | | ALL | |
| 152S00726 | 152S00592 | | ALL | |
| 376S1053 | 376S0604 | | ALL | Diodes alt to Fairchild |
| 353S00636 | 353S4037 | | ALL | |
| 155S00007 | 155S0667 | | ALL | |
| 376S1106 | 376S0678 | | ALL | Fairchild alt to Vishay |
| 371S00127 | 371S00182 | | ALL | |
| 152S00769 | 152S00659 | | ALL | |
| 372S00016 | 372S00015 | | ALL | |
| 107S00041 | 107S00039 | | ALL | |
| 740S00041 | 740S0159 | | ALL | |
| 311S00138 | 311S0436 | | ALL | |
| 152S00725 | 152S00590 | | ALL | |
| 152S00841 | 152S00238 | | ALL | |
| 376S00219 | 376S00079 | | ALL | TI for Fairchild |
| 311S00121 | 311S0398 | | ALL | |
| 311S0596 | 311S0593 | | ALL | |
| 353S3526 | 353S3528 | | ALL | |
| 353S3527 | 353S3528 | | ALL | |
| 197S00131 | 197S00116 | | ALL | |
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| 197S00115 | 197S00116 | | ALL | |
| 152S00398 | 152S00204 | | ALL | |
| 152S00786 | 152S00344 | | ALL | |
| 311S00165 | 311S00164 | | ALL | |
| 128S00050 | 128S0351 | | ALL | |
| 138S00047 | 138S00073 | | ALL | |
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| 155S0665 | 155S00232 | | ALL | |
| 740S00051 | 740S00050 | | ALL | |
| 152S00724 | 152S00311 | | ALL | |
| 155S0694 | 155S0387 | | ALL | |
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| 740S0144 | 740S0118 | | ALL | |
| 740S00028 | 740S0118 | | ALL | |
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| 138S00093 | 138S00035 | | ALL | |
| 138S00056 | 138S1100 | | ALL | |
| 107S00015 | 107S00011 | | ALL | |
| 152S00543 | 152S00484 | | ALL | |
| 155S00018 | 155S0664 | | ALL | Murata w/ Taiyo |
| 152S00359 | 152S00253 | | ALL | Chillisin alt to Cyntec |
| 311S00118 | 311S0489 | | ALL | |
| 155S00365 | 155S00191 | | ALL | |
| 107S00070 | 107S0085 | | ALL | |
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| 353S01346 | 353S01320 | | ALL | |
| 376S00281 | 376S1147 | | ALL | |
| 376S00230 | 376S00174 | | ALL | |
| 128S00022 | 128S00018 | | ALL | |
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| 107S0248 | 107S0250 | | ALL | |
| 107S00033 | 107S00034 | | ALL | |
| 107S00103 | 107S00058 | | ALL | Cyntec w/ Yageo |
| 311S00013 | 311S0508 | | ALL | Part wi |
| 132S00064 | 132S0409 | | ALL | |
| 128S0364 | 128S0264 | | ALL | Kemet w/ Panasonic |
| 128S00058 | 128S00018 | | ALL | NEC w/ Rohm |
| 107S00071 | 107S00053 | | ALL | |
| 376S00014 | 376S0761 | | ALL | |
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| 107S00044 | 107S00076 | | ALL | |
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| 128S00070 | 128S00007 | | ALL | |
| 740S00019 | 740S00007 | | ALL | Bourns w/ Polytronics |
| 353S00852 | 353S4262 | | ALL | TI w/ OnSemi |
| 138S0775 | 138S0860 | | ALL | |
| 138S0789 | 138S0941 | | ALL | Murata w/ SS |
| 152S00363 | 152S00048 | | ALL | |
| 152S00415 | 152S00140 | | ALL | |
| 155S00204 | 155S0731 | | ALL | |
| 311S00060 | 311S0273 | | ALL | |
| 128S00009 | 128S00007 | | ALL | |
| 138S0738 | 138S1101 | | ALL | Samsung alt to Murata |
| 107S00234 | 107S00235 | | ALL | |
| 311S00156 | 311S00129 | | ALL | |
| 155S0660 | 155S0513 | | ALL | |
| 197S00120 | 197S00118 | | ALL | |
| 152S00368 | 152S00269 | | ALL | |
| 311S0271 | 311S00008 | | ALL | NXP w/ Diodes |
| 311S00104 | 311S00091 | | ALL | |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 128S00039 | 128S00038 | | ALL | |
| 128S0302 | 128S00038 | | ALL | |
| 138S1103 | 138S0719 | | ALL | |
| 376S00074 | 376S0855 | | ALL | |
| 311S00180 | 311S00181 | | ALL | |
| 152S00770 | 152S0857 | | ALL | |
| 740S00033 | 740S00002 | | ALL | |
| 155S00166 | 155S0391 | | ALL | |
| 107S0249 | 107S0251 | | ALL | |
| 155S00401 | 155S00067 | | ALL | |
| 152S00369 | 152S00268 | | ALL | Cyntec w/ NEC |
| 371S00074 | 371S0602 | | ALL | |
| 138S0689 | 138S0701 | | ALL | |
| 128S00087 | 128S00011 | | ALL | |
| 128S00031 | 128S00011 | | ALL | |
| 128S00026 | 128S00011 | | ALL | |
| 152S00182 | 152S00703 | | ALL | |
| 152S00705 | 152S00412 | | ALL | |
| 376S00303 | 376S00012 | | ALL | |
| 152S00864 | 152S00851 | | ALL | |
| 311S00179 | 311S00166 | | ALL | |
| 353S01505 | 353S01389 | | ALL | |
| 353S01506 | 353S01404 | | ALL | |
| 311S00057 | 311S0612 | | ALL | |
| 377S0155 | 377S0184 | | ALL | |
| 152S00403 | 152S00322 | | ALL | |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 103S00248 | 103S00247 | | ALL | 8.06K 0.1% RESISTOR |
| 103S00250 | 103S00249 | | ALL | 18.2K 0.1% RESISTOR |
| 116S00006 | 116S0175 | | ALL | 0OHM RESISTOR |
| 128S00062 | 128S00067 | | ALL | 150UF POLY CAP |
| 128S00069 | 128S00067 | | ALL | 150UF POLY CAP |
| 128S00065 | 128S00067 | | ALL | 150UF POLY CAP |
| 138S00097 | 138S0750 | | ALL | 4.7UF CAP |
| 131S00134 | 131S00041 | | ALL | 12pF Desense:31561601 |
| 107S00101 | 107S00005 | | ALL | 5mOhm :31560708 |
| 107S00087 | 107S00029 | | ALL | 5mOhm :31560843 |
| 107S00086 | 107S00056 | | ALL | 3mOhm : 31560937 |
| 107S00100 | 107S00057 | | ALL | 2mOhm : 31561063 |
| 107S0240 | 107S0255 | | ALL | 1mOhm : 31561401 |
| 107S00139 | 107S0178 | | ALL | 220KOhm :31561213 |
| 128S0296 | 128S0487 | | ALL | 47uF-PT : 31561532 |
| 128S00012 | 128S0487 | | ALL | 47uF-PT : 31561532 |
| 138S0786 | 138S0705 | | ALL | Murata w/ Samsung |
| 353S00832 | 353S00525 | | ALL | IMVP SA |
| 353S00831 | 353S00519 | | ALL | IMVP VCORE |
| 152S00782 | 152SS00772 | | ALL | IMVP CORE INDUCTOR |
| 138S00105 | 138S00037 | | ALL | 10uF CER : 31563978 |
| 138S0714 | 138S0713 | | ALL | 10UF : 31564912 |
| 138S0648 | 138S0703 | | ALL | 4.7uF CER : 31564224 |
| 138S0715 | 138S0732 | | ALL | 1UF CER : 31565015 |
| 152S00845 | 152S00815 | | ALL | |
| 138S00111 | 138S00036 | | ALL | 20uF CER : 31563894 |
| 132S00012 | 132S0401 | | ALL | 0.22uF : 31563715 |
| 138S00084 | 138S00060 | | ALL | 47uF CER : 31564055 |
| 138S0739 | 138S0706 | | ALL | NEC w/ Vishay |
| 138S0945 | 138S0706 | | ALL | NEC w/ Rohm |
| 138S0641 | 138S0700 | | ALL | Murata w/ SS&Taiyo |
| 138S0759 | 138S0762 | | ALL | |
| 138S00049 | 138S0831 | | ALL | |
| 107S00090 | 107S00055 | | ALL | |
| 138S0863 | 138S0853 | | ALL | |
| 138S00006 | 138S0835 | | ALL | |
| 377S0077 | 377S0183 | | ALL | |
| 371S00180 | 371S00077 | | ALL | NXP alt to Diodes |
| 138S00104 | 138S0978 | | ALL | |
| 138S00024 | 138S0986 | | ALL | |
| 152S0434 | 152S1829 | | ALL | |
| 197S00053 | 197S00050 | | ALL | Kyocera w/ TXC |
| 197S00054 | 197S00050 | | ALL | NDK w/ TXC |
| 197S00055 | 197S00050 | | ALL | Murata w/ TXC |
| 335S00270 | 335S00203 | | ALL | Adesto for Micronix |
| 155S00034 | 155S0706 | | ALL | Taiyo w/ Murata |
| 353S00879 | 353S00754 | | ALL | |
| 155S00203 | 155S0894 | | ALL | |
| 152S00461 | 152S00112 | | ALL | |
| 376S00146 | 376S1061 | | ALL | |
| 152S00704 | 152S00413 | | ALL | |
| 152S00199 | 152S00413 | | ALL | |
| 335S00066 | 335S0946 | | ALL | |
| 372S0186 | 372S0185 | | ALL | |
| 311S00177 | 311S00178 | | ALL | |
| 353S00750 | 353S00877 | | ALL | |
| 152S00707 | 152S00689 | | ALL | |
| 376S00282 | 376S1128 | | ALL | |

VRAM ALT SUB-BOMS

| | | | | |
|---|---|---|---|---|
| 685-00222 | 685-00221 | | ALL | |
| 685-00223 | 685-00221 | | ALL | |
| 685-00224 | 685-00221 | | ALL | |
| 685-00225 | 685-00221 | | ALL | |

| | | | | |
|---|---|---|---|---|
| 311S0426 | 311S00007 | | ALL | |
| 138S00229 | 138S00107 | | ALL | |
| 353S01614 | 353S4159 | | ALL | |
| 132S00202 | 132S00175 | | ALL | |

| | | | | |
|---|---|---|---|---|
| 311S00193 | 311S00192 | | ALL | |
| 371S00170 | 371S00125 | | ALL | |
| 376S00302 | 376S1038 | | ALL | |

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PAGE TITLE

BOM Alt Table

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DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 147 OF 200

PAGE

SHEET 130 OF 131

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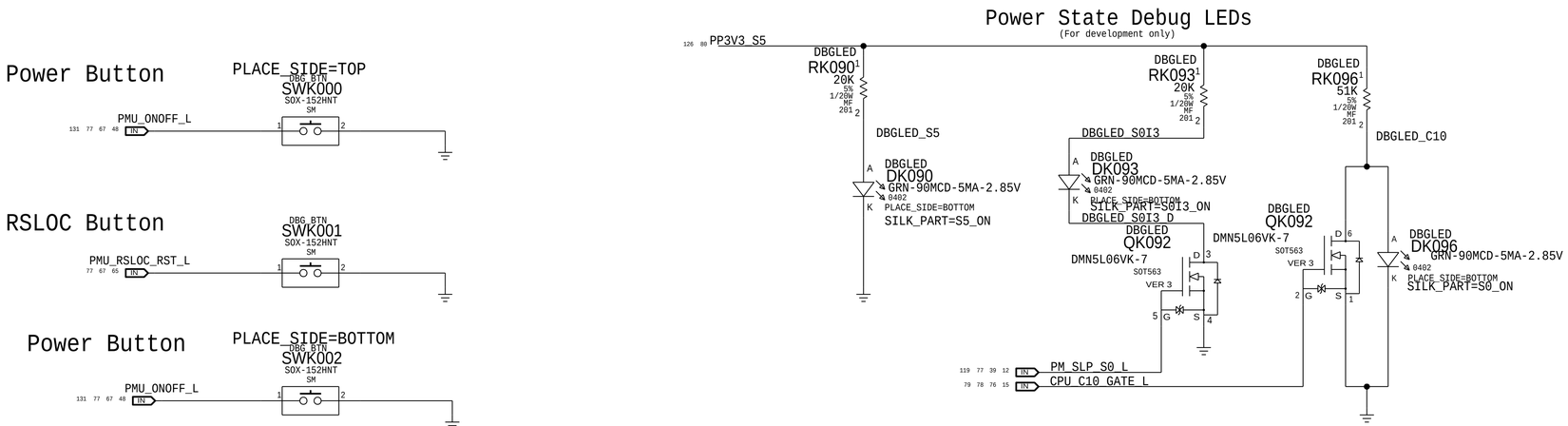
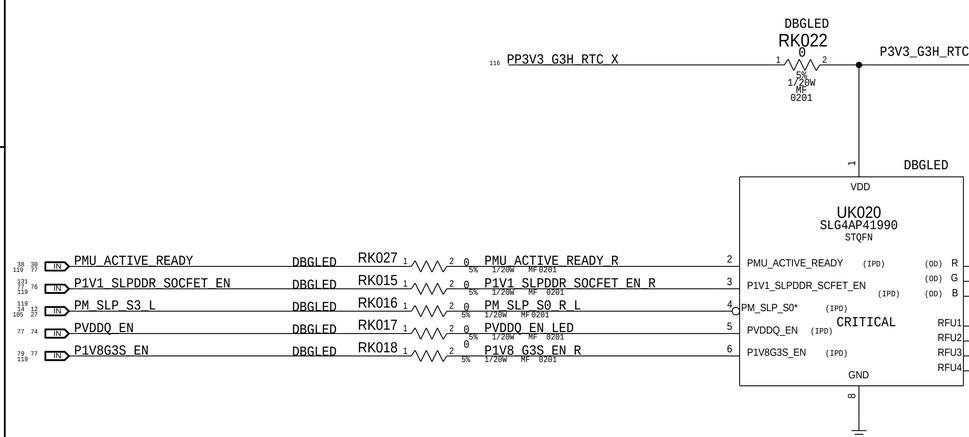



## System State LEDs

| INPUT | | | | | OUTPUT | | |
|---|---|---|---|---|---|---|---|
| PMU_ACT_RDY | SLP_SCFET_EN | SLP_S0_L | VDDQ_EN | 1V8G3S_EN | R | G | B |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |




## SOC State LEDs

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ADITYA SYNC_DATE=03/22/2017

PAGE TITLE
Dev Support

Apple Inc.

DRAWING NUMBER 051-02888 SIZE D

REVISION 1.0.0 EVT

BRANCH 200 OF 200

PAGE

SHEET 131 OF 131

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